COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY
1977

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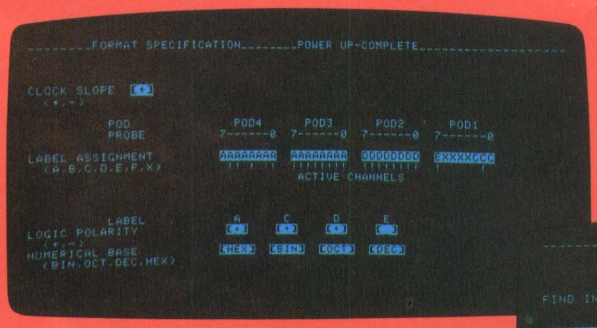
At last...a Logic State Analyzer that practically asks you what to analyze and how to display.

A few simple pushbuttons, an interactive display, sophisticated microprocessor-based intelligence . . . now they're all combined in HP's powerful new 1610A Logic State Analyzer. The result is a simplified "menu" approach to instrument setup, ability to choose highly complex trace specifications with a few simple keyboard entries, program-flow displays that are easier than ever to interpret, and an instrument that virtually self tests.

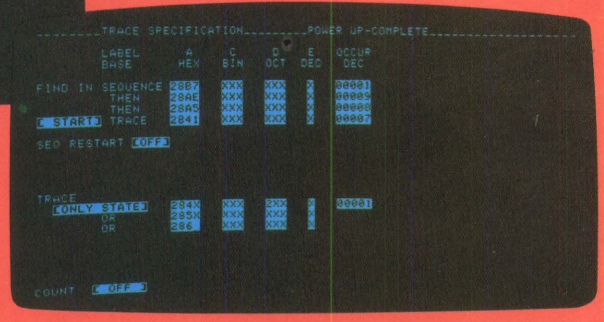
In addition, now you can trace complex branches and nested loops; count the number of states or the time interval between two words to debug or optimize programming; and drive HP Model 9866A or 9866B printers for hard-copy output of test results and set-up specifications.

The new 1610A, priced at $9500*, provides fast setup and easy trouble-shooting in nearly any logic system having data rates to 10 MHz. Your local HP field engineer has the complete story. Give him a call today.

* Domestic U.S.A. price only.

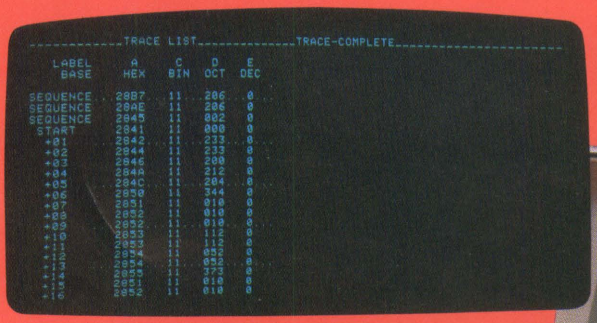


Setup ease. Inverse-video fields and moveable cursor in Format Specification mode direct you in defining clock slope, positive or negative logic and display formats (Hex, Binary, Octal or Decimal). You can also assign alphabetic labels to groups of data bits acting as a unit, greatly simplifying setups and display formatting. In addition, the display verifies probe-lead continuity and signals node activity.



Complex measurement capability. Fields and moveable cursor in Trace Specification mode simplify selection of trigger conditions and trace qualifiers. The ability to define up to seven sequential 32-bit words makes it possible to trace a specific path in complex branched programs. For further conditioning you can define the number of times each sequential state is to occur to allow the analyzing of looped or nested loop programs. And you can define up to seven states or groups of states for selective trace, simplifying data analysis and reducing the need for deep memory.

Simplified interpretation. List Display shows you trigger words plus the program flow you specified in the set-up specifications. Now you can easily compare operating software to original source listings or, in the trace-compare mode, to program flow stored in the 1610A memory.



System overview. Graph Display, showing data magnitude (y axis) vs. time for all 64 words in memory, gives you a system overview. Keyboard entries establish upper and lower y-axis scale values, and moveable intensified dots let you select specific areas for list display.



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087/13

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- A position arm anticipatory sensing system.

An exclusive Kennedy feature, the linear, non-contact (Mag Pot) position sensor requires no lamp source and assures performance for the life of the machine.

- Interchangeable electronics on all Series 9000 transports, reduce stocking costs and down time.
- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick-release hubs.
- All models are available with either 7 or 9 track, 800 NRZI, 1600 PE or 800/1600 NRZI/PE.
- 7 and 9 track NRZI and PE format/ control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available.

Series 9000's performance is as impressive as its features, with data transfer rates to 72KHz, and tape speeds from 10 to 45 ips.

Series 9000 is the hottest digital tape transport series around, and we plan to keep it that way, with constant improvements, rigid quality control and greater service capabilities. That should give you a warm feeling if you have a requirement for digital tape transports.

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CIRCLE 2 ON INQUIRY CARD



Tally reliability. As good as gold.

Tally reliability is unmatched in the printer industry. The value to you is a 100% duty cycle, 200 line per minute printer that costs far less to own. Less than any other printer around.

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The reason behind this unparalleled reliability is the patented Tally print comb mechanism. It uses a unique flexure technology that's impervious to wear and designed for unlimited life. While other printers like to talk about calculated MTBF, Tally points to field proven MTBF. Most of the Tally printers that have been in the field, including those in operation for over four years, have never required adjustment or repair to the print mechanism. In fact, many have experienced no malfunction at all! No one else can safely make that statement. And Tally backs every T-2000 with a full year print mechanism warranty.

The gold printer above is Tally's commemorative unit marking 10,000 machines delivered. The noteworthy statistic is that 99 per cent plus have never had a mechanism failure.

Find out all the facts on this proven performer and call your nearest Tally sales office, or write or call Tally Corporation, 8301 S. 180th Street, Kent, WA 98031. Phone (206) 251-5524.

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CIRCLE 3 ON INQUIRY CARD

THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

JULY 1977 • VOLUME 16 • NUMBER 7

FEATURES

64 **IFIP CONGRESS 77**
The international triennial gathering of the International Federation for Information Processing, Congress 77 emphasizes applications, networks, and computer systems technology with a technical program of over 100 sessions, and an exhibition of products and services pertaining to the field of information processing

77 **AN INTEGRAL REAL-TIME EXECUTIVE FOR MICROCOMPUTERS**
by Kenneth Burgett and Edward F. O'Neil
Optimized real-time software for single-board microcomputer systems, based on analysis of primary performance characteristics, permits inexpensive system modifications to meet changing requirements

85 **TIMING PECULIARITIES OF MULTIPLEXED RAMs**
by J. Reese Brown, Jr
While 16-pin 4k RAMs provide advantages of smaller package size, fewer required drivers, and better pinouts, their timing cycles are complex. Knowledge of their dynamic differences prevents users from encountering serious operational difficulties

95 **TIME SLICING OFFERS AN ALTERNATIVE TO MULTIPROCESSOR SYSTEMS**
by Janak Pathak
Multitasking under control of a single microprocessor using time-slicing techniques obtains modularity advantages of multiprocessors while maintaining design simplicity of single processor systems

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by David Herberg, Nirmal Ratnakumar, and Peter E. Lobban
A programmable microprocessor controller can automate the control of processing steps involved in the epitaxial growth of silicon for ICs by adjusting gas flow rates

146 **PRINTER/PLOTTER IS PRICE-COMPATIBLE WITH MICROPROCESSOR SYSTEMS**
By employing the user's software for control and by incorporating simple equipment design features, this peripheral attains a low cost/performance ratio that is consistent with that of microprocessor-based systems

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BPA **CIRCULATION OVER 55,000**

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Why Does Intel Love Lucy?
...and our M-10A Memory & LSI Test Systems?

Besides being fun to talk to, Lucy Beyer has something to say about Memory and LSI Test Systems. Here's what she says about our customer Intel Memory Systems. Intel has purchased 21 of our M-10A Memory Test Systems. Here's what they got!

- Whether debugging a new design or testing memory boards or systems on the floor, Micro Control's system gets the job done fast . . . with automatic Schmoo plots & error mapping (software supplied).
- Reduced labor costs because of Micro Control's help gets products to customers faster at less cost.
- Powerful, flexible address and data generators in the M-10A test complex logic functions . . . byte control, parity, asynchronous control, even LSI.
- Real time error logging, even at the memory systems level.
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- Lots of other things, not the least of which is the $39K starting price (Intel compared M-10A with $80K machines but purchased ours!) All M-10A and M-10AT Systems include: Training, First-line component design, Same-day service, Design changes for customer convenience, and Extensive Software!

Lucy Beyer, Sales Administrator, Micro Control Company. Call Lucy at (612) 786-8750 collect! She might refer you to Harold Hamilton, (he's not as much fun, but you can't have everything).



MICRO CONTROL COMPANY

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CALENDAR

CONFERENCES

JULY 24-29—ISA Sym for Innovation in Measurement Science, Hobart/Smith College, Geneva, NY. INFORMATION: Peter Vestal, Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

JULY 28-29—ACM-Pacific 77 (Assoc for Computing Regional Conf), San Jose, Calif. INFORMATION: Peter Szego, Ampex Corp, M/S 3-22, 401 Broadway, Redwood City, CA 94063. Tel: (415) 367-3126

AUG 4-6—Personal Computing Fair, Boston U, Boston, Mass. INFORMATION: Personal Computing Fair, Boston University Summer Term, 725 Comm Ave, Boston, MA 02215. Tel: (617) 731-2326

AUG 8-12—IFIP Congress 77 (Internat'l Federation for Information Processing), Toronto, Canada. INFORMATION: Robert C. Speiker, U.S. Committee for IFIP Congress 77, Western Electric Co, 222 Broadway, New York, NY 10038

AUG 23-26—Internat'l Conf on Parallel Processing, Bellaire, Mich. INFORMATION: Dr Charles S. Elliot, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812

SEPT 6-8—7th Internat'l Congress on Instrumentation in Aerospace Simulation Facilities, Royal Military College of Science, Shrivenham Wiltshire, England. INFORMATION: Gen'l Chm, 7th ICIASF, P. W. W. Fuller, R31 RARDE, Fort Halstead, Sevenoaks, Kent, England

SEPT 6-9—COMPCON Fall (IEEE Computer Soc Internat'l Conf), Mayflower Hotel, Washington, DC. INFORMATION: COMPCON Fall '77, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

SEPT 6-10—INELTEC '77, U.S. Computer and Peripheral Catalog Exhibition, Basel, Switzerland. INFORMATION: U.S. Dept of Commerce, Domestic and Internat'l Business Administration, Catalog Exhibition Section, Washington, DC 20230. Tel: (202) 377-3973

SEPT 19-21—WESCON (Western Electronic Show and Convention), San Francisco, Calif. INFORMATION: William C. Weber Jr, Gen'l Mgr, WESCON, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (800) 421-6816

SEPT 26-28—Internat'l Electrical Electronics Conf and Exhibition, Toronto, Canada. INFORMATION: Internat'l Electrical Electronics Conf and Exposition, 1450 Don Mills Rd, Don Mills M3B 2X7, Canada

SEPT 26-28—Distributed Computer Control Systems Internat'l, University of Aston, Birmingham, England. INFORMATION: IEE, Savoy Place, London WC2R OBL, England

SEPT 27-29—Military Electronics Defense Expo 77, Wiesbaden, West Germany. INFORMATION: Joseph Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

OCT 3-6—EUROMICRO Sym, Amsterdam, The Netherlands. INFORMATION: Ted Holtwijk, Philips Elcoma, Bldg BAE 2, NL-Eindhoven, The Netherlands

OCT 6-8—3rd Internat'l Conf on Very Large Data Bases, Tokyo, Japan. INFORMATION: James Gabbert, MIT Sloan School, 50 Memorial Dr, Rm E53-330, Cambridge, MA 02139

OCT 6-12—Stockholm Internat'l Technical Fair, Stockholm, Sweden. INFORMATION: Radley Communications Ltd, 509 Madison Ave, New York, NY 10022. Tel: (212) 838-9215

OCT 9-15—INTELCOM 77 (Internat'l Telecommunications Exposition), Atlanta, Ga. INFORMATION: Barbara Coffin, Promotion Mgr, Horizon House Internat'l, 610 Washington St, Dedham, MA 02026. Tel: 1-800-225-9977, (617) 326-8220

OCT 10-13—10th Conv of Electrical and Electronic Engineers in Israel, Tel Aviv, Israel. INFORMATION: Daphna Knassim, Ltd, 444 Madison Ave, New York, NY 10022. Tel: (212) 688-7072

OCT 17-20—ISA/77 (Instrument Society of America Conf & Exhibit), Internat'l Conv Ctr, Niagara Falls, NY. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

OCT 18-20—Internat'l Conf on Modeling Semiconductor Devices, Lausanne, Switzerland. INFORMATION: Secrétariat des Journées d'électronique, Dept d'électricité-EPFL, 16 chemin de Bellerive, CH-1007 Lausanne, Switzerland

OCT 19-20—10th Annual Electronic Connector Sym, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014

OCT 25-27—Semiconductor Test Sym, Cherry Hill, NJ. INFORMATION: Mrs R. J. Sunderland, Secretary and Registrar, Test Symposium Committee, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 424-2400

OCT 31-NOV 2—AIAA/IEEE/NASA Computers in Aerospace, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Hugh Harrington, Dept E411, McDonnell Douglas Astronautics, PO Box 516, St Louis, MO 63166. Tel: (314) 232-9102

NOV 7-11—Electronic Components 77, U.S. Trade Ctr, London, England. INFORMATION: Robert Connan, Office of Internat'l Marketing, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3465

NOV 8-10—Compec UK 77 (Computer Peripherals Exhibition), Wembley Centre, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1- 9LU, England

SEMINARS

AUG 22-23—New Products: A Systematic Approach, New York University, School of Cont Educ, New York City. INFORMATION: Heidi Kaplan, Information Services Mgr, New York Conf Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

OCT 3-6—Fifth Internat'l Purdue Workshop on Industrial Computer Systems, Purdue U, West Lafayette, Ind. INFORMATION: Dr T. J. Williams, 102 Michael Golden, Purdue U, West Lafayette, IN 47907

SHORT COURSES

AUG 1-3 and OCT 17-19—Microcomputer Systems Design, Buffalo, NY. INFORMATION: Dr Hinrich R. Martens, Prof of Electrical and Mechanical Engineering, State University of New York at Buffalo, 3435 Main St, Buffalo, NY 14214. Tel: (716) 831-3211

AUG 1-5—Semiconductor Memories—Principles and Applications, Milwaukee, Wis. INFORMATION: John T. Snedeker, Program Director, U of Wisconsin-Ext, Dept of Engineering, Civic Center Campus, 929 N 6th St, Milwaukee, WI 53203. Tel: (414) 224-4193

AUG 1-5—Data Communications Systems and Networks; SEPT 19-23—Advances in Electronics Technology; SEPT 26-30—Small Computer Systems, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

AUG 22-26—Computer Control of Processes, U of Colorado, Boulder. INFORMATION: Center for Management and Technical Programs, U of Colorado, PO Box 3253, Boulder, CO 80307. Tel: (303) 492-8356

SEPT 12-22—Data Communication, Iowa State U, Ames. INFORMATION: Data Communications Conf, 331 Coover Hall, Iowa State University, Ames, IA 50011. Tel: (515) 294-4777



One company can cut keyboard costs. Even when their keyboards cost more.

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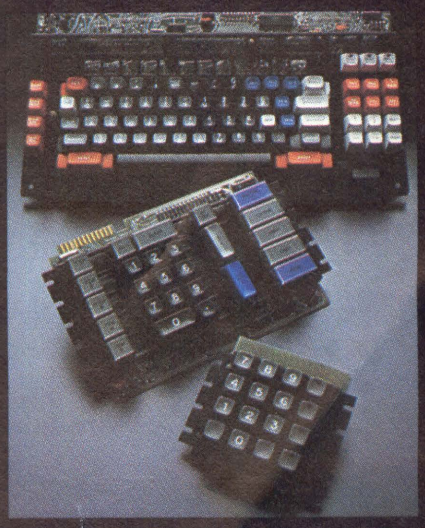
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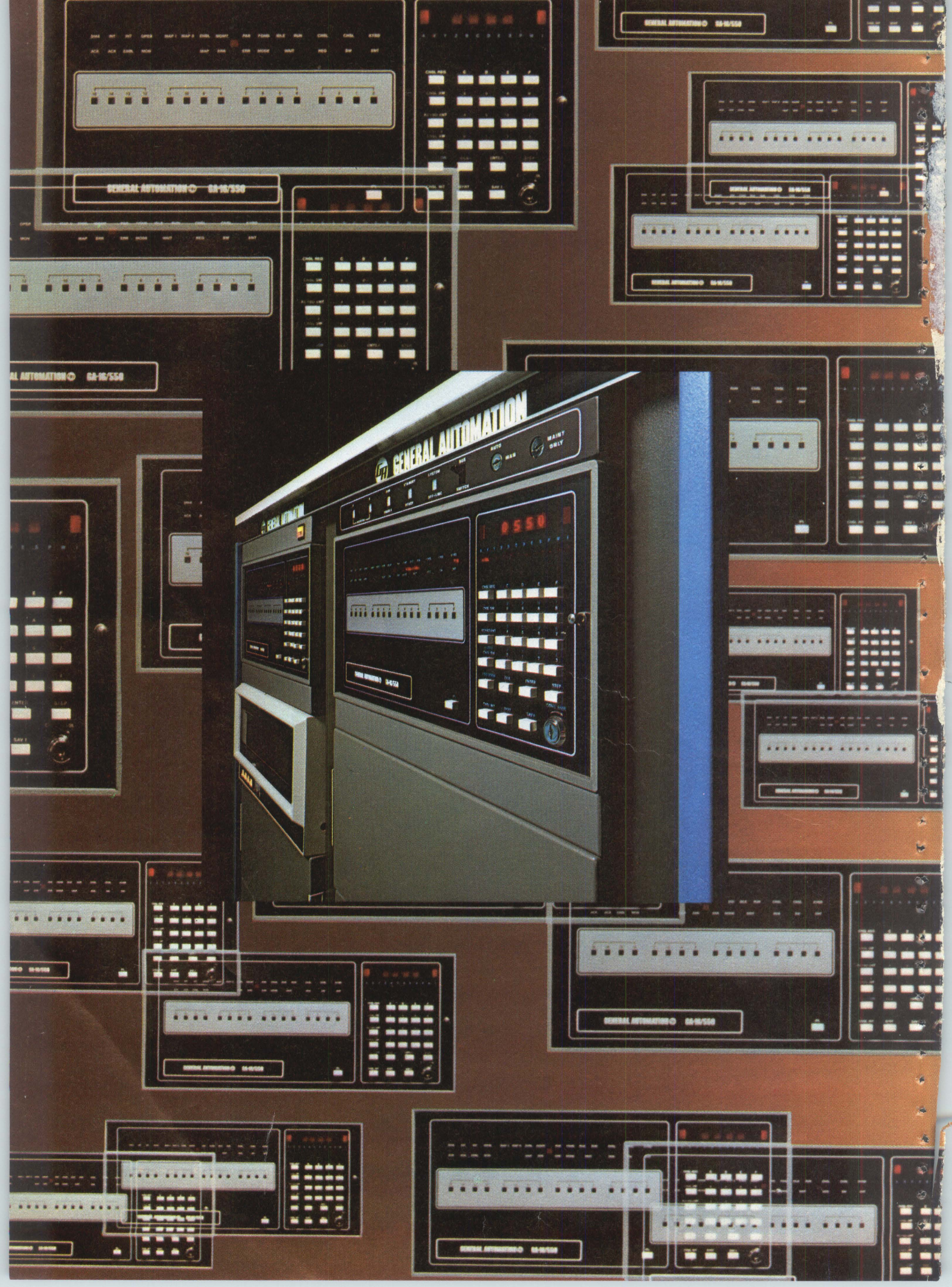
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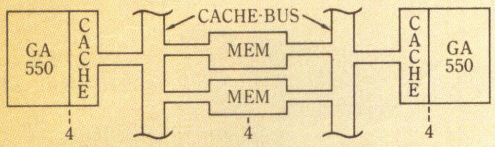

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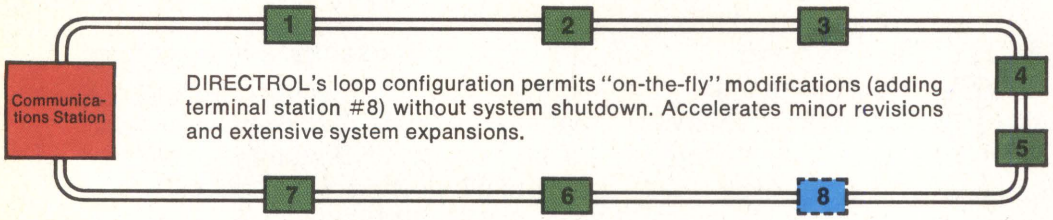
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CD-6

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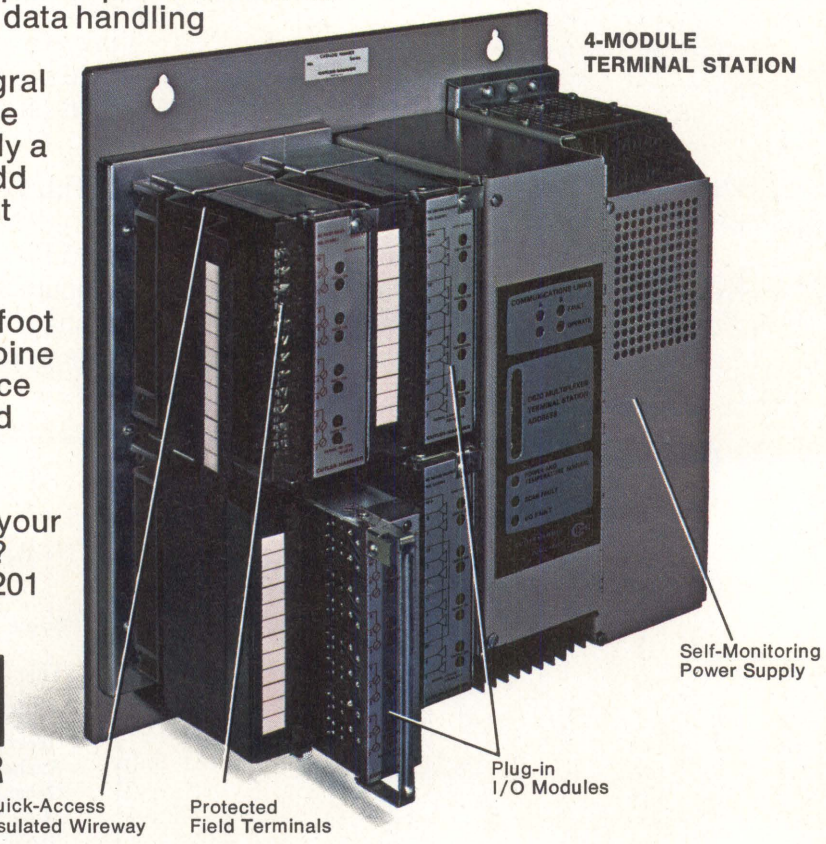
DIRECTROL's loop configuration permits "on-the-fly" modifications (adding terminal station #8) without system shutdown. Accelerates minor revisions and extensive system expansions.

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Ramifications of the Revised WATS Tariff

Possible outcome of the anticipated major revision of the AT&T WATS Tariff (FCC Tariff No 259), pertinent to both voice and data communications system users from two perspectives, has previously been considered (*Computer Design*, "Communication Channel," Feb 1977, pp 14, 18, and Mar 1977, pp 12, 14). The Wide Area Telecommunication Service (WATS) is undoubtedly the service which is most widely used by U.S. business other than direct distance dialing (toll). While it would be difficult to definitely establish the total actual savings realized by this wide spectrum of WATS users, it is universally agreed that the largest amount of total direct dollar savings is from this area. The second significant aspect of this tariff filing is the fact that since 1974 the realizable direct savings from proper WATS usage has been progressively diminished by the intended design of the WATS rate structures. The level of saving of a typical WATS user in 1974 was 40 to 60% greater than in 1977 for the same network, calling usage volume, and distributions. This reduction in savings potential is even more dramatic for the shorter distance WATS user, ie, band 1 WATS network only.

The recent WATS tariffs and associated policies implemented by AT&T have further complicated the ability of the WATS user to properly manage his network for maximum calling value. The institution of maximum utilization on a full business day (FBD) WATS line as well as the minimum average call length billing criteria has impacted the calling value of sharing an FBD WATS network between administrative daytime voice calls and night data communications calls by the company's computer system. The communications common carrier presently refuses to provide any total utilization and calls data for FBD WATS lines; such data are readily available to the local billing telephone company. The WATS user is therefore unable to verify the value of the FBD WATS lines or, in the case of WATS simulated groups, to determine if all the billed WATS lines were actually operational. The communications common carrier attempts to provide the absolute minimum information of actual WATS usage to the user. An example is provided by charges the telephone companies impose on a WATS user for a detailed record on magnetic tape or punched cards of each WATS call. While such charges vary among telephone companies they universally tend to be more punitive than compensatory.

This continued handicapping of a user's WATS administration capability is also supported by the nonavailability of any calling detail for an Inward WATS network, since the compilation of such data provides no billing and hence revenue advantages to the telephone companies. This lack prevents proper administration of the network and therefore improves the probability that misuse will occur, typically resulting in higher WATS billings than necessary.

WATS provides the largest accumulated calling saving by virtue of the great number of users. Coupled with the continual eroding of WATS network alternatives and value management capabilities, as reflected in the proposed WATS tariff, it is most important that this latest revenue producing mechanism be thoroughly understood.

AT&T has filed its latest interstate WATS tariff. Based on the required minimum examination period of 90 days, the rates and policies are anticipated to become effective on August 1, 1977 unless delayed by FCC action, even though this filing was prompted by an FCC directive to AT&T to correct discriminatory WATS rate structures. Overpricing of WATS to the shorter distance user (bands 1 and 2) which comprise the majority of WATS networks had been indicated by the FCC. The revised WATS tariff however does not clearly indicate a responsive reply to that FCC directive.

The tariff divides the continental U.S. into three bands instead of the previous five. The relationships between the old and new geographic delineations are as follows:

Old WATS		New WATS
Band 1 Area	=	Band A-1 Area
Bands 2, 3, and 4 Areas	=	Band A-2 Area
Band 5 Area	=	Band A-3 Area

The FBD WATS line which provided maximum opportunity for calling savings has been eliminated. All lines are now measured time (MT) only. The user who was able to properly control and manage his FBD WATS network to produce high per line utilization levels was rewarded by significant calling cost savings. Under the revised tariff, this user will experience a significant increase in monthly charges.

Even though all WATS lines will be MT lines, the illusion of a savings possibility has been structured into the tariff. The present MT WATS tariff provides a mini-

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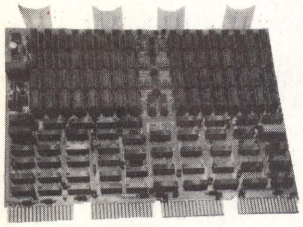
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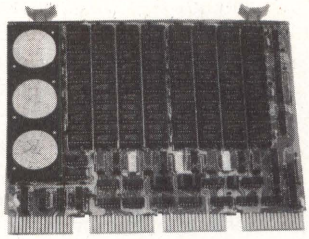
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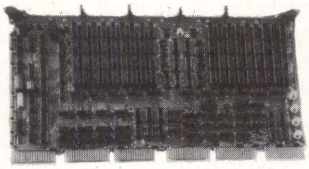
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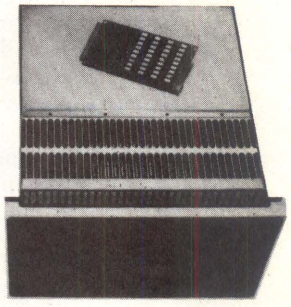
More reliable than disk or comparable core memory.

Nonvolatile with available battery backup.

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April

PDP-11/70 Memory

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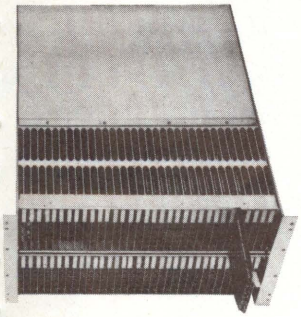
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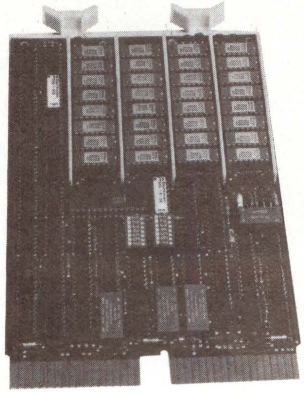
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MSC 4601
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CIRCLE 13 ON INQUIRY CARD **CIRCLE 14 ON INQUIRY CARD**

TABLE 1

Proposed Outward WATS Rates from New York City

Band	Initial Period 0 to 10	Overtime 1 Next 30 h 11 to 40	Overtime 2 Next 50 h 41 to 90	Overtime 3 Next 50 h 91 to 140	Overtime 4 Next 60 h 141 to 200	Overtime 5 All Hours Over 201 to 744
	$	$/h	$/h	$/h	$/h	$/h
A-1	213.00	11.85	9.38	2.38	1.60	0.76
A-2	246.00	14.72	11.66	8.48	1.98	0.99
A-3	270.00	16.95	13.42	9.77	2.29	1.09

mum charge for the first 10 hours of monthly usage and a lower additional per hour charge for utilization beyond that time. The future tariff maintains the monthly minimum charge per line concept but has a declining per hour charge for utilization beyond that minimum period. In increments of 30- and then 50-hour segments, the per hour charge for additional WATS utilization is reduced.

As shown in Table 1, the user of this WATS tariff initially assumes that to achieve the lowest per hour rate, calling usage must be concentrated on as few WATS lines as possible. With the present WATS, this characteristic has resulted in networks comprised of a few FBD WATS lines that are supplemented with one or two MT lines. During slack or normal calling periods only the FBD WATS lines are accessible through operator or under computerized PBX control. When peak periods develop by virtue of predicted time periods or an increase in the number of queued calls, the MT WATS lines are activated. Such a WATS network design and operation provides maximum calling savings, without adversely compromising the grade of service required by the calling personnel.

Structure of the revised tariff apparently realizes these cost saving techniques and has therefore decreed that WATS billing will be based on the average line usage within the same service group. This not only destroys many effective WATS network design techniques to improve savings but also eliminates any single WATS line accountability by the telephone companies. If a WATS service group comprises five WATS lines, such as shown in Table 2, and one FBD line was sporadically malfunctioning, the telephone company would be liable for a billing adjustment if such a condition were detected by the WATS user. With the proposed line averaging such billing adjustments will be virtually impossible to obtain even though such a condition may have caused excessive toll costs.

The typical practice of merely adding a few MT WATS lines to the end of a WATS service group as an assurance of obtaining the best grade of service may only slightly

TABLE 2

Proposed WATS Tariff Cost Analysis WATS Group Loading

Present WATS Tariff

Lines	Minutes	Cost for Band 1	Cost for Band 5
Line 1 (FBD)	8000	$900.00	$1675.00
Line 2 (FBD)	6500	900.00	1675.00
Line 3	4500	900.00 (FBD)	1439.70 (MT)
Line 4 (MT)	3000	784.00	980.20
Line 5 (MT)	1500	416.50	520.70
	Totals	3900.50	6290.60

Proposed WATS Tariff

Total WATS Minutes	23,500 minutes	
Average WATS Line	4,700 minutes	
	Band 1	Band 5
Average WATS Line Cost	$928.70	$1292.49
Total WATS Line Cost	$4643.50	$6462.45
Cost Increase	$743.00 (19.1%)	$171.85 (2.7%)

TABLE 3

Proposed WATS Tariff Cost Analysis WATS Misloading

Assume: Band 5 FBD WATS line with 6000 min total usage including 1000 min of band 1 calls

	Cost
Under Present WATS Tariff:	
Band 1 calls	None
Under Proposed WATS Tariff:	
Direct band 1 calling	$187.62





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CIRCLE 15 ON INQUIRY CARD

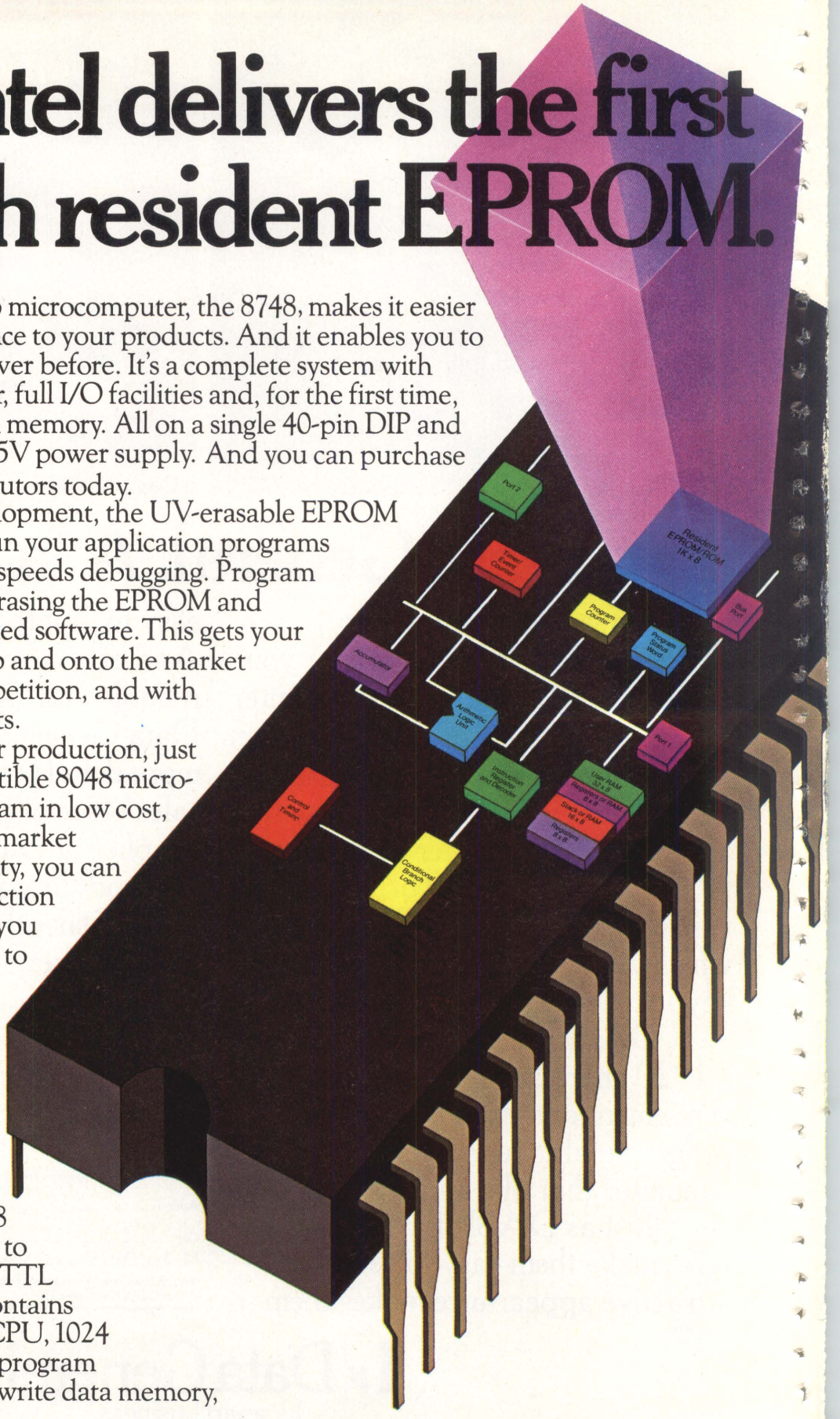
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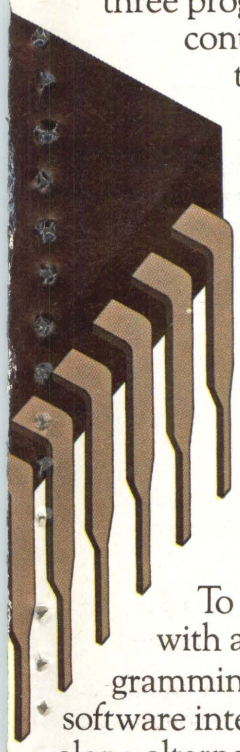
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single chip microcomputer The 8748.



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There's also a new 8035 microcomputer that is exactly like the 8748/8048 but without resident program memory. It enables you to precisely match system memory size to your needs, using external ROM or EPROM.

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8048	Single chip μC with 1K bytes masked ROM	NOW
8035	Single chip μC without resident program memory	NOW
8243	I/O Expander with 16 high current drive I/O lines	NOW
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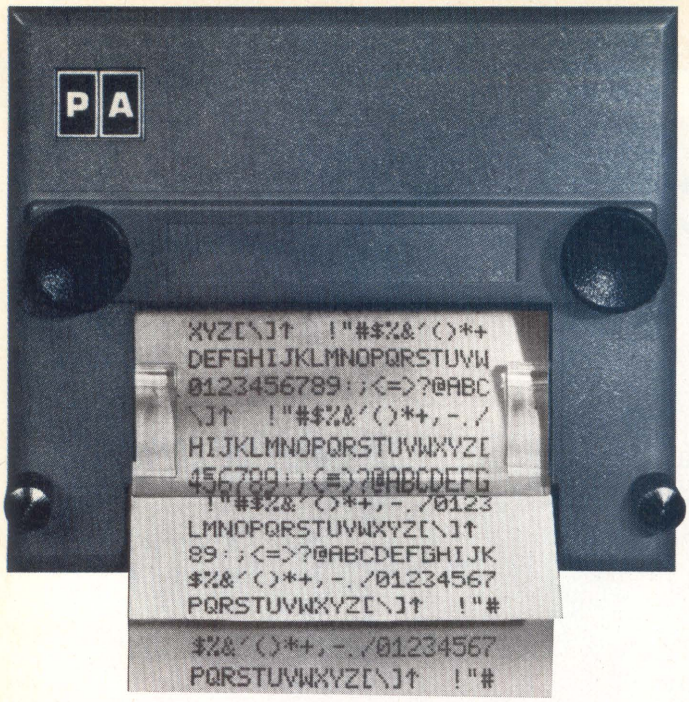
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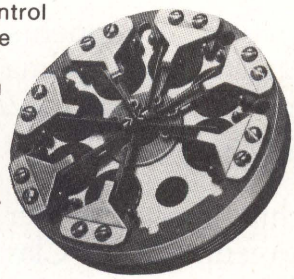


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impact the realized savings with the present WATS tariffs. Under the revised tariff, continuation of this practice will be a major revenue source to telephone companies.

Table 2 illustrates a typical WATS service group and the associated costs under the present and proposed WATS tariffs. It also shows that the shorter distance WATS user is again about to experience the maximum economic impact.

The existence of FBD WATS lines has created certain practices of WATS line loading. If an FBD band 5 WATS line was producing savings with band 5 calling volume, the use of that line for band 1 calls was considered a good management practice providing these band 1 calls did not block a legitimate band 5 call. Such a case would be an East Coast company that would use the band 5 FBD WATS lines in the earlier business morning hours (9 to 11 am) for band 1 calls until the West Coast business day began. Table 3 presents an example of the continuing value of this practice.

In summary, the revised WATS tariff further restricts the ability of the communications manager to design a WATS network and procedures to meet the organization's calling characteristics while still producing maximum savings. It also reduces the accountability of telephone companies. Those WATS users who are presently using the WATS tariff in an inefficient and costly manner will experience the least financial impact from this new tariff. Unfortunately, those users who have properly designed their networks and carefully controlled the call loadings to realize the maximum calling savings are about to be rewarded with a severe economic impact.

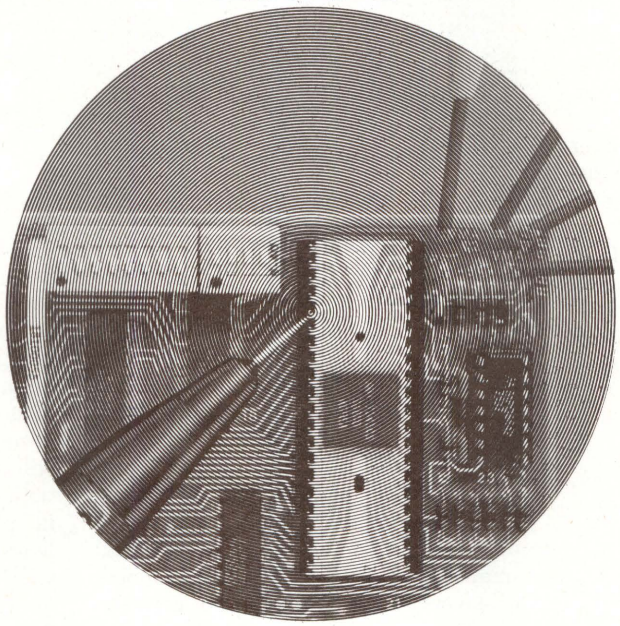
In order to obtain the maximum communications value with the advent of this WATS tariff, a number of areas must be considered. Most importantly, the communications network designer must be more careful in considering the economic justification of using tie lines and foreign exchange lines to eliminate these calling concentrations from the network. The revised WATS networks should only be used for those calls that cannot be placed by means of the private line tariff services. An increase in the number of different private line applications, however, will increase the complexity of personnel calling procedures which typically increases the incidents of nonprocedural compliance and calling misuse.

It is also extremely important that a minimum number of WATS lines be established in each WATS service group due to the line averaging provision of the tariff. Present practices of using longer distance FBD WATS for shorter distance calls during non-peak periods now becomes a most costly practice. The need for independently provided call usage data will become even more important in attempting to achieve and maintain optimum calling value, that is, lowest calling cost with a compatible grade of service.

Fortunately, the more sophisticated communications manager can now offset the threatened penalties of this tariff by the application of computerized telephone systems. Such systems that provide automatic call routing, call queuing, station identification, and call recording by individual trunk can arm the communication user with the ability to adjust to and minimize the penalties inherent in this and future communications tariffs. These capabilities supported by resulting management and analysis data offer the only hope for continued cost effective communications. The value and application of the emerging computerized telephone system in permitting tangible control of these increasing calling costs will be explored in next month's column.

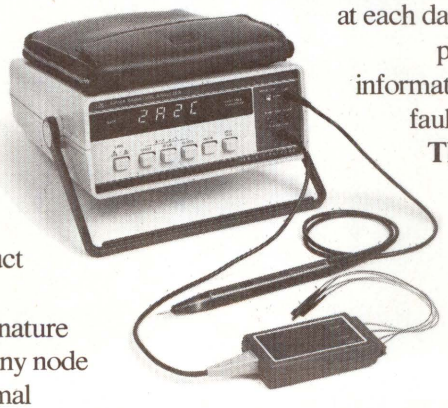
CIRCLE 17 ON INQUIRY CARD

Troubleshoot microprocessor products fast–



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CIRCLE 18 ON INQUIRY CARD

Testing Has Begun of Glass Fibers For Optical Communications

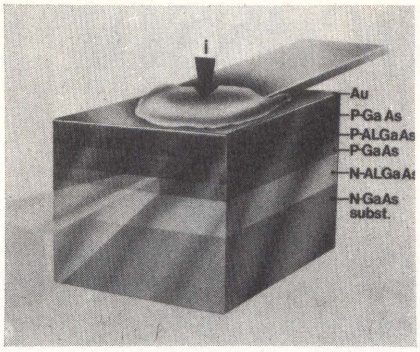
Preparations are underway for testing of optical communication systems in which copper wires and coaxial conductors are replaced by fine glass fibers. Large transmission capacity, smaller dimensions, lighter weight, and immunity to electromagnetic interference, known advantages of fiber cables, are expected to meet increasing telecommunications uses, some of which require large bandwidths.

A testing facility is being built in the Project Centre of Philips Research Laboratories in Geldrop, The Netherlands, in cooperation with Telecommunications and Defense Systems Div and the Glass Div of Philips. The transmission capacity of the 6-fiber cable is 140M bits/s/fiber, corresponding to 1920 telephone channels/fiber. To achieve this rate, the semiconductor laser light source has to be switched on and off at least 140M times/s. The light detector must transform these light pulses into electric pulses at the same rate.

Aim of the experimental system is to achieve a signal attenuation in the fiber of less than 5 dB/km, made possible with the aid of new fabrication methods. After each kilometer the signal is attenuated by less than a factor of 0.7. A repeater amplifier will be set halfway in the cable (at 8 km) to regenerate the signal back to its original intensity.

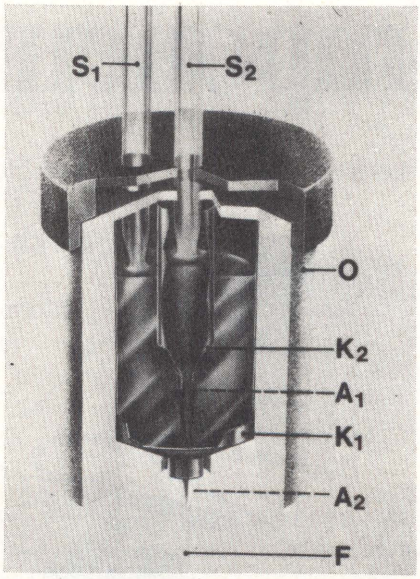
Glass fibers can be made from both soda glass and quartz-glass (fused silica). Both feature optimum properties of little loss of light from the fiber surface during transmission, little loss of light due to absorption through the fiber. and maximum maintenance of the shape of the light pulses over large distances.

In the fabrication of soda glass, two glass melts are used; the glass with the larger refractive index forms the core of the fiber. The glasses mix somewhat as they are drawn from the crucible, giving fibers of 100 μm in diameter with the desired refractive index profile. In the other method, hundreds of extremely thin quartz-glass films from a plasma are deposited onto the inside wall of a fused silica tube, providing the desired profile of the refractive index. The tube is heated so that it collapses to a solid rod; fibers with an outer diameter of 100 μm are then drawn from this rod. Once fabricated, the fibers of either glass are clad with a plastic coating for protection and mechanical reinforcement.



Schematic drawing of semiconductor laser shows various layers (not to scale). When electric current (i) is passed through, laser emits almost monochromatic radiation

Dimensions of the semiconductor laser are comparable to the diameter of the fiber. Power consumption is small. Lasers are built up of a number of layers, such as of mixed crystals of aluminum gallium arsenide, on a gallium arsenide substrate. Laboratory life of experimental lasers has been increased to about 20,000 hours. Future lasers are expected to achieve 100,000 hours, the minimum requirement for an optical communication system.



Double-crucible apparatus for drawing of fibers of soda glass (schematic). K_1 and K_2 are concentric crucibles of pure platinum. They are heated in electric furnace 0 to a suitable temperature so that glasses melt. Glasses are fed in from two preformed rods of pure glasses S_1 and S_2 of different refractive indices. As glasses are drawn out, a slight mixing takes place over the traject A_1A_2; this gives the desired profile in the refractive index of the fiber

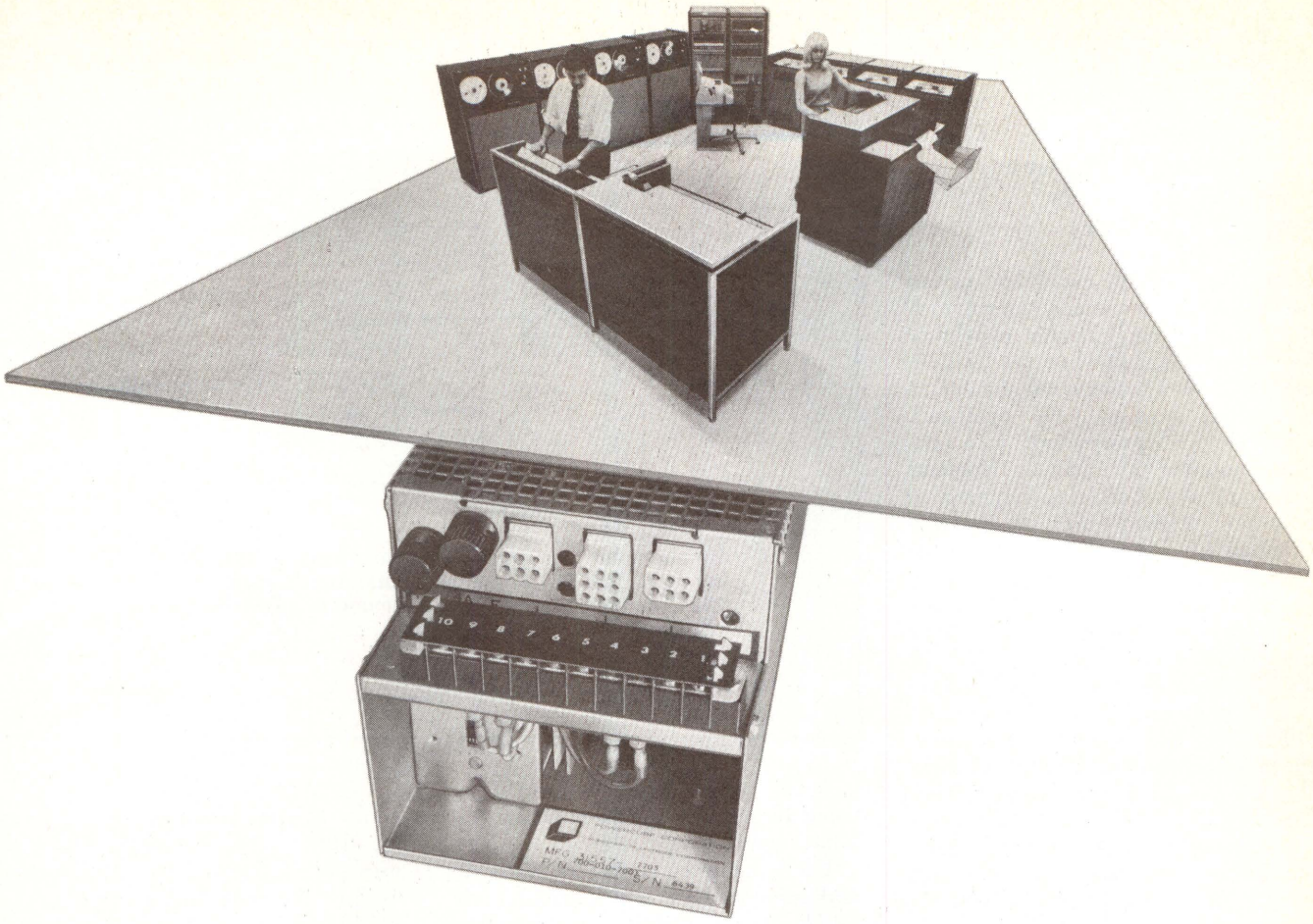
Precision required for coupling two fibers or a fiber and detector is already adequate. However, higher precision is necessary for coupling the light source to the fiber. A device has been devised to facilitate this operation—the laser and fiber are placed on micromanipulators and positioned to within 0.2 μm before being clamped. This aligns the laser so that it shines along the fiber nearly as axially as possible.

The laboratory testing facility is being built in steps. First is a single 6-km glass fiber containing one repeater halfway. Next, a cable of the same length, but with six glass fibers, will be tested; it will be reinforced with tensioning wires and sheathed in plastic. The final cable with a length of 16 km is planned to be installed in 1978. By connecting all the fibers in series, with a repeater every 8 km only, the system can be tested over a total length of 96 km.

In another project aimed at testing the usefulness and reliability of this technique, an optical fiber cable of about 4 km in length is to be installed in the local telephone net in Berlin. This experimental cable will be used to transmit signals at a rate of 34M bits/s.

Lightwave Communications Are Being Evaluated In Full-Service Environment

Evaluation has been begun by Bell Systems, Chicago, Ill to analyze the feasibility of a lightwave communications system. Set up between two Illinois Bell switching offices, and between one of those facilities and a downtown Chicago office building, the system carries customers' voices, data, and video signals on pulses of light over a 1.5-mi (2.4-km) underground cable containing hair-thin glass fibers (see *Computer Design*, "Communication Channel," Mar 1977, p 18). A single pair of lightguides in the 0.5" (1.27-cm) diameter cable can carry 672 simultaneous conversations (at a 44.7M-bit/s rate) or an equivalent mix of voice and various types of data signals.



Powercube's new off-line switcher will hold you up for 50 milliseconds

Minicomputers, modems, microprocessor-based systems, multiplexers — whatever your application, you want reliability in your off-line switching power supply.

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Our new OLS Model 10 175-watt multiple-output series is designed for nominal input voltage of 115/230 VAC, 43 to 63 Hz. But it tolerates wide dynamic input fluctuations to assure continuous operation during "brown-out" conditions.

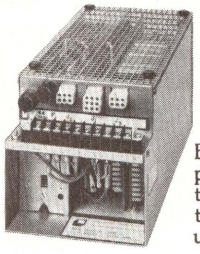
What's more, typical hold-up of output voltages is 50 ms at full load and nominal input, providing the longest possible housekeeping in anticipation of power failure.

And, there's more you ll like.

Borrowing on years of space-age power supply technology, Powercube has packaged this powerful unit in a compact, 5½" x 5½" x 11" envelope. You can use it almost anywhere. The OLS Model 10 is also 90% modular — a real time-saver when it comes to maintenance.

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CIRCLE 19 ON INQUIRY CARD

Hardware/Software Package Supports High Speed TTYs

Both slow and high speed devices can be combined on a single system with this terminal concentrator capability for more efficient line utilization, more than 50% lower communications costs, and reduced CPU overhead. Slow speed teleprinter-links to a central computer, as well as frontend hardware and processing required to support Teletype® terminals, are also eliminated. Designed for use on the company's PTS-100™ series of programmable terminal systems, the function package provides high speed capabilities in emulation of IBM 2260 and 3270 to Teletype terminals within data communications networks.

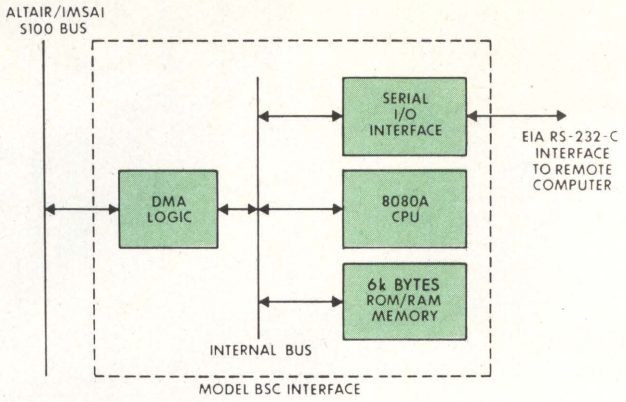
Keys to the capability from Raytheon Data Systems Co, Div of Raytheon Co, 1415 Boston-Providence Tpk, Norwood, MA 02062 are microprogrammable general-purpose communications adapters, each of which can control four half-duplex communications lines. Five adapters can be attached to each controller for concentrating messages from 20 lines and transmitting those messages to a host computer at rates of up to 7200 bits/s over the single, full-duplex line used to support 2260 or 3270 communications.

The terminal concentrator package controls the interchange of messages, reducing host message-buffering requirements. The number of low speed I/O connections at the host is also reduced, and the host addressing capability is increased. Basic package is able to support up to four Teletype terminal lines.

Circle 400 on Inquiry Card

8080/Bisync Interfaces Are Designed for Microcomputer Systems

Connections between the S-100 microcomputer bus and Bisync data communications protocol are possible with a family of synchronous data communication interfaces. Directly connecting a microcomputer system to standard IBM telecommunications hardware and software, each interface inserts in a standard IMSAI/Altair S-100 bus (two card slots); it communicates with a remote computer using Bisync protocol through an RS-232-C connection.



Synchronous data communication interface from Adtech connects the S-100 microcomputer bus through an RS-232-C connection, enabling communication with a remote computer using Bisync protocol

Each interface transfers data to and from its host microcomputer via DMA, thus requiring little programming effort. It also uses little of the host's processing power.

Interfaces are offered by Adtech, Inc, PO Box 10415, Honolulu, HI 96816. Model BSC-PP uses point-to-point Bisync (identical to that of the IBM 3780 system); BSC-POL uses polled Bisync (the same as that used by the IBM 3270 terminal); and BSC-HML utilizes HASP multileaving Bisync (such as is used in various RJE workstations). A fourth, capable of SDLC communications, will also be offered.

Circle 401 on Inquiry Card

Bankwire Systems to Use µProcessor Terminals With 8B1 Protocol

Microprocessor-controlled stations consisting of 10-char/s EDT 33s and 30-char/s EDT 300s, programmed for Bell System 8B1 protocol, will be used in Bankwire II, a private-wire data communication system for commercial banks. Payment and Telecommunication Services Corp has signed a contract with Western Union Data Services Co for the terminals. Eight teleprinter station arrangements have been made available. Terminals will operate on ac or dc hubbed facilities; those with ASR (automatic send-receive) arrangements will be able to set up format controls on paper tape loops.

The microprocessor controller in each station arrangement controls transmission and reception of traffic to and from a Collins 8562 computer system. Features include full-duplex operation, terminal identification capabilities for security, and error detection. The protocol permits the computer to poll all terminals selectively or in sequence.

National Data Network Transmits Over Phantom Circuits

In order to be able to cope with an anticipated rapid expansion in remote data processing, the Deutsche Bundespost (DBP) has begun setting up a national data network to cover the whole of the Federal Republic of Germany by the end of 1978. Recently handed over to the DBP, the initial section of the network is being set up between Frankfurt and Mannheim by Siemens AG, D-8000 München 1, Postfach 103, Germany.

Transmission medium is the long-haul cable 17a. To transmit data over the phantom circuits of the symmet-

CIRCLE 20 ON INQUIRY CARD →

Guess who's helping OEMs and system builders get out in front of their competition?

Honeywell's Level 6 Minicomputer is helping OEMs and systems builders stay ahead of the pack.

With its fully open-ended architecture and unique Megabus that lets you mix processors, memories, communications, and peripherals to meet just about any systems requirement.

With versatility that offers tabletop, rack-mounted, and office versions.

With software that includes GCOS 6/MDT, a Multi-Dimensional Tasking disk-based operating system that provides multi-tasking for independent on-line processing concurrent with batch or program development. It features an indexed-sequential file access method and supports multiple real-time or data communications applications in multiple streams.

With program preparation aids that include a powerful Text Editor; FORTRAN, COBOL and RPG compilers; and a wide range of utilities and debugging aids.

With our attractive OEM pricing, contracts and policies.

And with a worldwide mainframe supplier on your team, when you need maintenance or support, you don't have to hunt for it.

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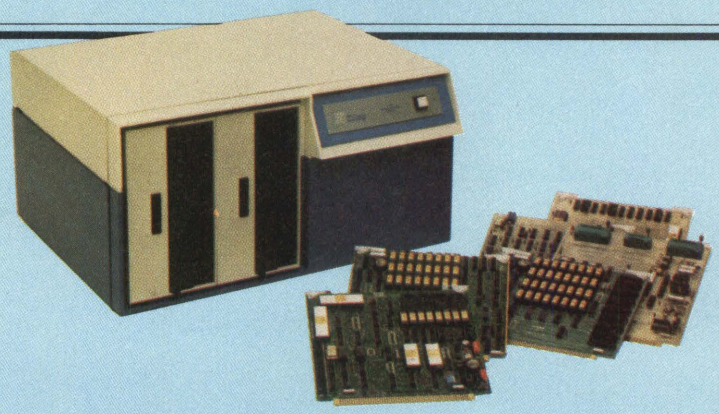
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Zilog introduces the first Z-80 disk based microcomputer system.

The Z-80 MCS Microcomputer—designed to be the most advanced general purpose microcomputer available today. You get massive computing power at a price so low you'll find it most difficult to believe.





A bold new weapon is Zilog's breakthrough Microcomputer System.

It's a general purpose unit that gives users high performance at remarkably low cost—and it features all the reliability and low maintenance you have come to expect—and get—from Zilog.

Just for starters consider these Z-80 MCS system features.

- Full use of the powerful Z-80 CPU with its 158 instruction set, considered to be the most advanced in the industry.
- Main memory storage capacity of up to 64K bytes of RAM, PROM or EPROM. The standard basic system comes with 3K bytes PROM and 16K bytes of dynamic memory.
- Dual floppy disks with 600,000 bytes of storage.
- RS-232 or current loop serial interface for communication with a CRT or TTY. And room is available to add more.
- Two parallel I/O ports for simple interface to other peripherals, and more ports are available.

And a nine slot card cage, housed along with everything else in a heavy duty metal chassis, allows the Z-80 MCS the expansion capability and flexibility you need for design options. And you get a full complement of expansion cards. Read on.

Standard software ready for development.

With the MCS you get a PROM Based Monitor. A Macro Assembler, File Maintenance, Editor, Debug and Utility Routines are also part of the standard package.

Available options: BASIC. MCS/RIO with relocating assembler and linking loader. And coming soon a powerful repertoire of programs including MCS-COBOL and PLZ.

Needless to say complete documentation and system support comes along as part of the package.

Get unprecedented power thanks to the Z-80 MCS internal architecture.

Not only does it include all of the instructions of the preceeding processors, but goes far beyond.

Memory Block moves. Up to 65K bytes can be moved at the rate of 8.4 microseconds per byte.

Memory Block searches. The entire memory of the system can be searched with a single instruction.

Block I/O operations. I/O transfers at rates of up to 125 kilobytes/second can be accomplished under software control.

Bit Handling. Any bit in any register or memory location can be set, tested or cleared with a single instruction.

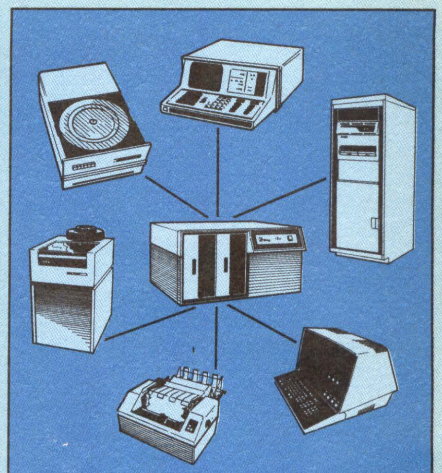
Relative Jumps. Short, two-byte relative control transfers reduce program sizes. Three-byte absolute jumps provide access to any memory location.

Eight and sixteen bit arithmetic operations provide fast data and address calculations. BCD arithmetic and shifting is also supported.

Plug in these cards to further expand the Z-80 MCS's capabilities.

- RMB: contains 16K bytes of RAM consisting of 4K dynamic RAM devices.
- IOB: allows you to expand the system by four I/O ports per board.
- SIB: allows you to add 4 Serial RS-232 ports per card.
- PMB: contains 16 sockets for additional PROM Memory per board.

Configure the MCS the way you want it.



8 connector slots let you add a variety of peripherals such as CRT, printers, paper punches, etc. It's your choice.

This is all a part of our pledge.

That pledge, to stay a generation ahead is further demonstrated by the new Zilog MCS. We urge you to learn more and a suitable brochure has been prepared. It can be yours, just write or call.

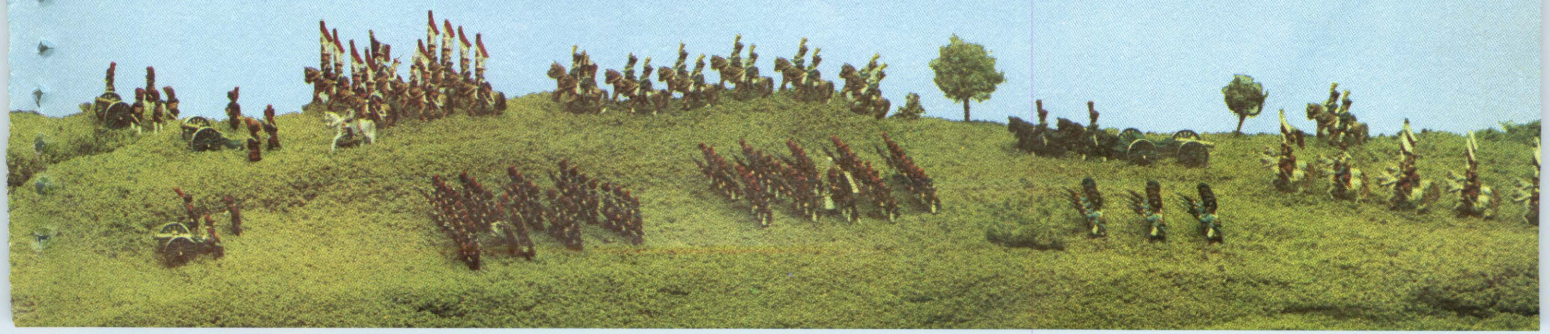
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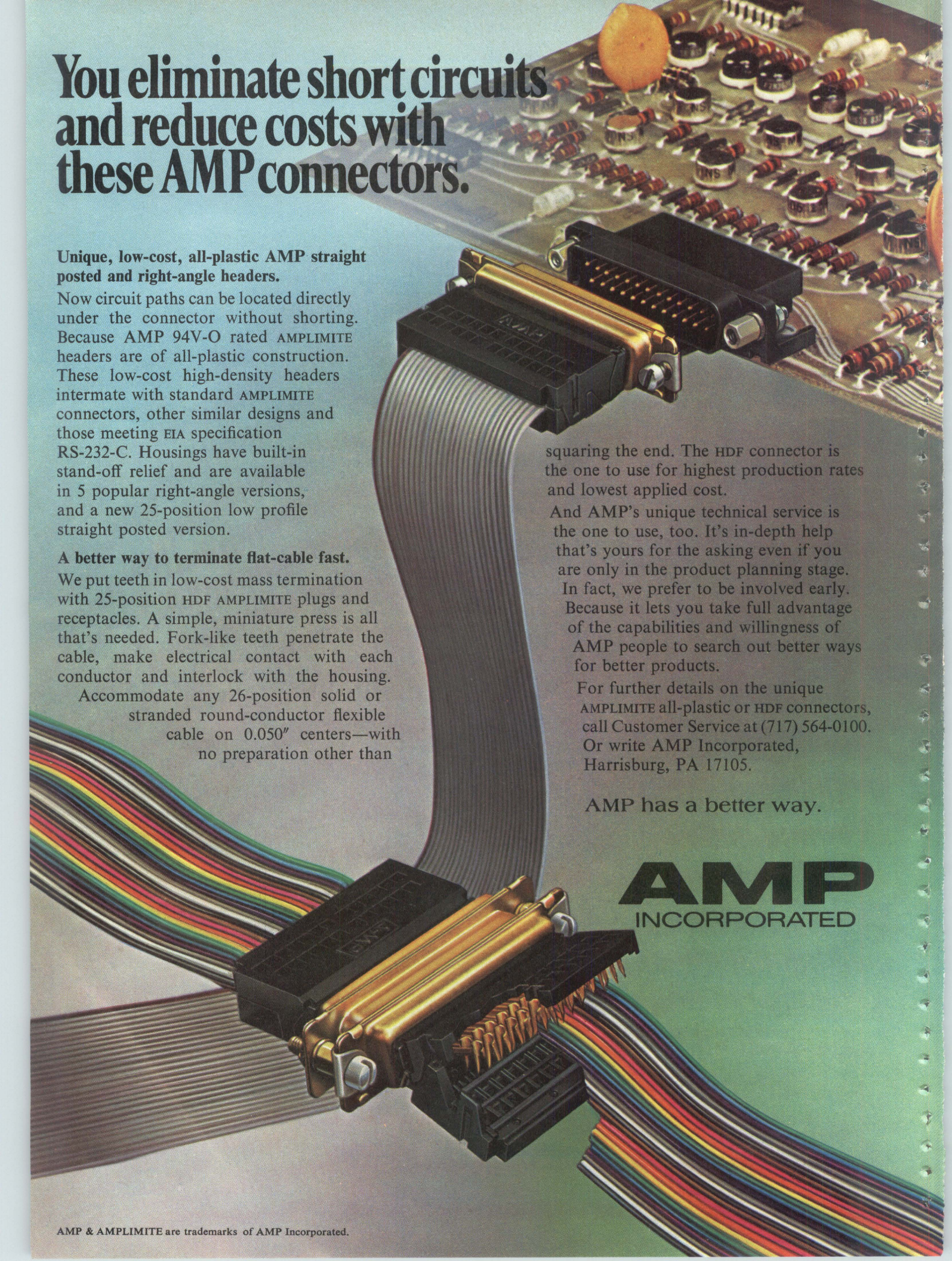
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CIRCLE 21 ON INQUIRY CARD

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You eliminate short circuits and reduce costs with these AMP connectors.



Unique, low-cost, all-plastic AMP straight posted and right-angle headers.

Now circuit paths can be located directly under the connector without shorting. Because AMP 94V-O rated AMPLIMITE headers are of all-plastic construction. These low-cost high-density headers intermate with standard AMPLIMITE connectors, other similar designs and those meeting EIA specification RS-232-C. Housings have built-in stand-off relief and are available in 5 popular right-angle versions, and a new 25-position low profile straight posted version.

A better way to terminate flat-cable fast.

We put teeth in low-cost mass termination with 25-position HDF AMPLIMITE plugs and receptacles. A simple, miniature press is all that's needed. Fork-like teeth penetrate the cable, make electrical contact with each conductor and interlock with the housing. Accommodate any 26-position solid or stranded round-conductor flexible cable on 0.050″ centers—with no preparation other than squaring the end. The HDF connector is the one to use for highest production rates and lowest applied cost.

And AMP's unique technical service is the one to use, too. It's in-depth help that's yours for the asking even if you are only in the product planning stage. In fact, we prefer to be involved early. Because it lets you take full advantage of the capabilities and willingness of AMP people to search out better ways for better products.

For further details on the unique AMPLIMITE all-plastic or HDF connectors, call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

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CIRCLE 22 ON INQUIRY CARD

rical conductor pair of this cable without impairing the 3000 long-distance telephone calls which are possible at the same time, Siemens and the DBP jointly developed the time-division multiplexed remote data transmission system PCM 30D. Its terminal groups up to 30 64k-bit/s data signals into a 2M-bit/s signal, transmitted over the phantom circuits in the 1- to 3-MHz frequency band.

To refresh pulses on the digital long-haul link, remotely fed regenerators are installed in repeater stations at 9-km intervals. A maximum of 17 regenerator sections make up a supervised section; both ends are terminated with line terminals with interface conversion function.

Network circuits are intended to interconnect telegraph and data switching centers of the EDS system, and to perform other remote data transmission tasks. Future expansion has been taken into consideration—a total of seven systems can operate over each existing transmission path without adding new cables.

Offering of Universal Data Transfer Service Is Finalized

According to ITT World Communications, Inc, 67 Broad St, New York, NY 10004, Telenet Communications Corp has concurred with its tariff for Universal Data Transfer Service, an international data communications service currently available between the U.S. and France, and the U.S. and Puerto Rico. The agreement will enable overseas users to access computer centers offering timesharing, data base, and information services on the Telenet domestic network. ITT Worldcom also has filed to provide this service to Belgium, Italy, and Spain, and plans to expand it to other countries.

Discount Plan Is Among Revisions Offered in Tariff Filing

A volume discount plan for its data communications public packet network is a key feature of tariff revisions which Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 filed with the Federal Communications Commission on April 25. Customers with monthly billings of over $5000 will pay a lower rate on charges above that amount. A majority of the new rates are scheduled to take effect on July 24. This will range from 20% discount on billings between $5000 and $9000, to 50% on billings over $18,000.

Also included is a restructuring of the 3-tier rate structure for public dial-in service to more closely reflect the costs of service. Rates of 10 high-density cities have increased, and 16 low-density city charges have been reduced; medium-density city rates remain unchanged.

Hot Line Data Service has been expanded to include stations operating at 50 to 110 bits/s and 1200 bits/s. Also featured is the upgrading of the Atlanta office to a major network switching center for the Southeast, enabling the accommodation of transmission speeds of up to 56k bits/s in that area.

Satellites Are Studied for Compatibility With NASA Space Shuttle

In a study funded by the National Aeronautics and Space Administration, researchers at Battelle's Columbus Laboratories, 505 King Ave, Columbus, OH 43201 are working with Ford Aerospace Communication Corp, General Electric Co's Space Div, RCA's Astro-Electronics Div, TRW, Inc, and Hughes Aircraft in a project to consider nine spacecraft. Results are intended to provide an analysis of SSUS design requirements for compatibility of satellites with the NASA Space Transportation System, a reusable Earth to orbit transport vehicle.

To achieve savings potential for the communications industry, NASA intends to develop a spinning solid upper stage (SSUS) to be deployed from the shuttle system. It would be able to carry a communications satellite into the desired orbit.

In addition, the study will provide detailed design information of the nine spacecraft in relation to missions currently projected by NASA for the 1980s. Criteria will be supplied to NASA's Marshall Space Flight Center, Huntsville, Alabama for contracting of system-definition phases for the SSUS. □

The 2900 Family: Two years later.

1975. Advanced Micro Devices introduces the world's best 4-bit microprocessor slice, the Am2901, along with a few support circuits.

1977. It's a whole new family. Now there's an Am2901A just like the Am2901, only better. Now there are 18 support circuits, two or three second sources and all the software you'd ever want. The 2900 family has become the family of the future. Here's why:

The first family.

The Am2900 family is the first group of products designed specifically for microprogrammed machines. Microprogramming is rapidly becoming the most popular way to design medium- and high-performance systems, to reduce development time, make changes easily, and conveniently add new features.

Less weight, less size.

With the Am2900 family, it's not uncommon for entire boards to be eliminated. You'll shrink system size and weight, increase overall reliability and reduce manufacturing costs.

Time goes by, price goes down.

In July 1975, we told you we'd reduce the cost of the Am2901 by 30% per year. We've done it twice. Once in April 1976 and once in March 1977. The Am2900 family gets less and less expensive all the time.

We're so popular, we're the industry standard.

The Am2900 family is the most widely used Bipolar LSI family in:

- Minicomputers: For emulators, high-performance CPU's and add-ons by eight out of the top ten U.S. manufacturers.
- High-performance controllers: For discs, tapes, floppy discs and universal controllers.
- Communications: For PBX systems, central exchanges, multiplexers and modems.
- Military: For radar processors, display systems and the Navy's new standard avionic computer, the AN/AYK-14.

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The Family:

CPU Slice (ALU and general registers)	Am2901A, 2902, 2903*, 2904*
Microprogram Control Units	Am2909, 2910*, 2911
Branch and Instruction Control for Microprogram Sequencers	Am29803, 29811
LSI Bus Interface Devices	Am2905, 2906, 2907, 2915A, 2916A, 2917A
Priority Interrupt Control	Am2913, 2914
Main Program Control	Am2930* 2931*, 2932*
New More Powerful MSI functions	Am2918, 2919, 2920 2921, 2922

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Plus:

Schottky and low-power Schottky MSI, MOS static and dynamic RAM's and all the devices you need to build your high-performance microcomputer.

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- A 16-Bit Microprogrammed Computer
- The Am2900K1 Learning and Evaluation Kit

The Microprogramming Handbook

- A High Performance Microprogrammed Disc Controller

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- Vertically Microprogrammed State Machines
- An emulation of the Am9080A/8224/8228 using the Am2900 family

And two terrific design aids:

AMDASM

Our powerful, easy-to-use microprogram assembler offering software support through the worldwide INFONET time-sharing division of Computer Science Corporation. (It supports user-defined mnemonics for producing microinstructions up to 128 bits wide, and includes formating and default features as well as tape generation for PROM programmers. If you've got the other guy's MDS system, ask for AMDASM/80. It comes on a floppy disk and runs under their operating system.)

AMDS

Beginning this fall, we'll be offering hardware support with the Advanced Microprogram Development System. (It's the first prototyping system especially designed for microprogramming systems.) It'll help speed up construction of prototype systems and generation and de-bug of microcode. Resident AMDASM, of course!

The Am2900 family.

It's today's product family for tomorrow's high-performance machines. Am2900. Remember that number. You're going to be hearing it a lot.

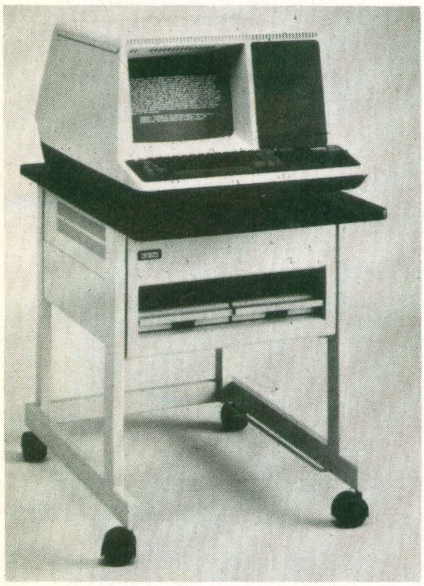
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Bipolar LSI. N-channel, silicon gate MOS. Low-power Schottky.
Multiple technologies. One product: excellence.



CIRCLE 23 ON INQUIRY CARD

Compact Computer System Integrates Single-Chip CPU With Video Display Unit



DECstation 78 provides user accessibility in a compact unit. Basic system incorporates LSI minicomputer in a design simplified by modular architecture

A compact, diskette-based unit, the DECstation™ 78 employs an LSI version of the PDP-8 minicomputer, the VT78 video data processor, integrated in a VT series video terminal, as its central element. Operating as a standalone computer system or as part of a network, the system, introduced by Digital Equipment Corp, Maynard, MA 01754, runs on 115 or 230 V, and can be assembled quickly through the use of plug-in components.

The minicomputer, a single-chip LSI (Intersil 6100) version of the PDP-8, is contained on a single hex-size board with internal CMOS ROM for system control. A second board holds 16k words of n-MOS RAM. Integral to the system are real-time clock, asynchronous communications, disc and high speed data interfaces, and electronic program injection using MR78 ROM capsules.

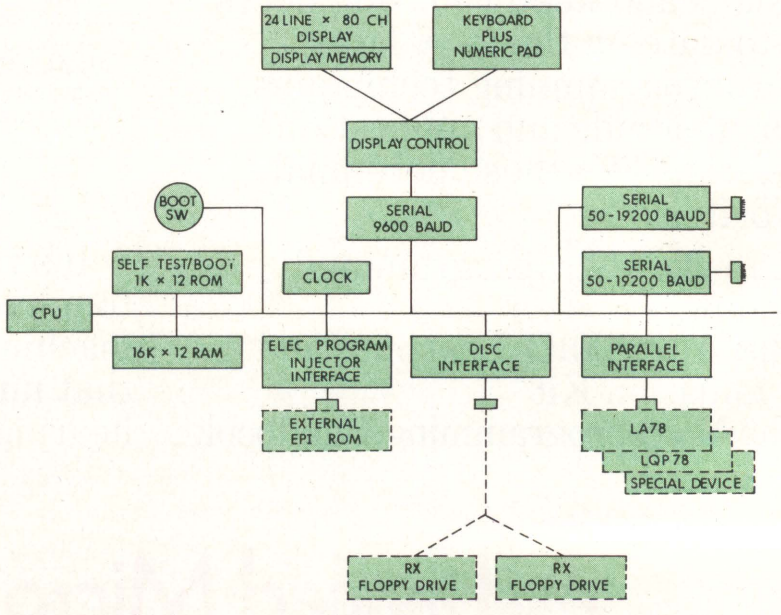
The display consists of a DECscope-type video terminal with alphabetic and numeric keypads, upper/lower case ASCII character set, 33 special symbols, and 19 user-defined special function keys. Mass storage is provided by RX78 dual diskette drives which function as a random-access file device, storing 256k 8-bit bytes/drive. Diskettes serve as a compact data interchange and software distribution medium. Hardcopy can be output on an LA78 DECprinter, which prints 132-col lines at up to 180 char/s.

External plug-in ports allow the user to adapt or reconfigure the system as needs change. The I/O connection panel on the back of the processor contains five ports. Two serial EIA RS-232-C asynchronous interface ports allow attachment of terminals and devices that operate from 50 to 19,200 baud. A parallel I/O port for printers and custom interfaces provides bidirectional 12-bit transfers at up to 15k words/s. A disc interface port allows connection to floppy disc units.

The fifth port accommodates the MR78 electronic program injection capsule. Designed to provide an inexpensive means of customizing the system for use in fixed function environments, the MR78 contains a load image of the desired program on ROM chips. A capsule is attached to the interconnect panel on the rear of the processor; when the start switch is pressed the program contained in the capsule is injected into main memory. Result is a low priced system for applications where diskette storage is not required.

Software includes both FORTRAN IV and BASIC compilers for high level program development. The DECstation operates under the OS/78 executive, which resides on floppy discs. The RTS/8 real-time monitor allows the unit to have real-time interfacing and to perform multitasking.

OS/78 is a single-user executive that permits program development, data storage, and numerical analyses to be performed on a standalone unit. It includes editing, assembly programs, language compilers, debugging facilities, and utility programs. Its logical interface to program and file



VT78 video data processor completely integrates the minicomputer and display of Digital Equipment Corp's DECstation 78. System CPU is a single-chip LSI version of the PDP-8 with 16k words of RAM

Compare the new Sanders Graphic 7 with other interactive terminals.



You'll draw a graphic conclusion.

Sanders' new Graphic 7 is an intelligent terminal with all necessary hardware and software as standard —not cost-you-extra—features.

But the Graphic 7 doesn't just save you money when you buy it. It also saves you money after you buy it.

Simply wheel your Graphic 7 through the door and plug it in. No installation problems.

Your programmer won't have to spend much time with your Graphic 7. It comes pre-programmed.

And your operators will be able to handle your Graphic 7 after a 10-minute briefing, because it works with a one-button initialize.

Application programs? Our Fortran-based graphic support package can reside in any host that supports Fortran.

And with the intelligence at the terminal, there's minimum impact on the host. You can do more work faster.

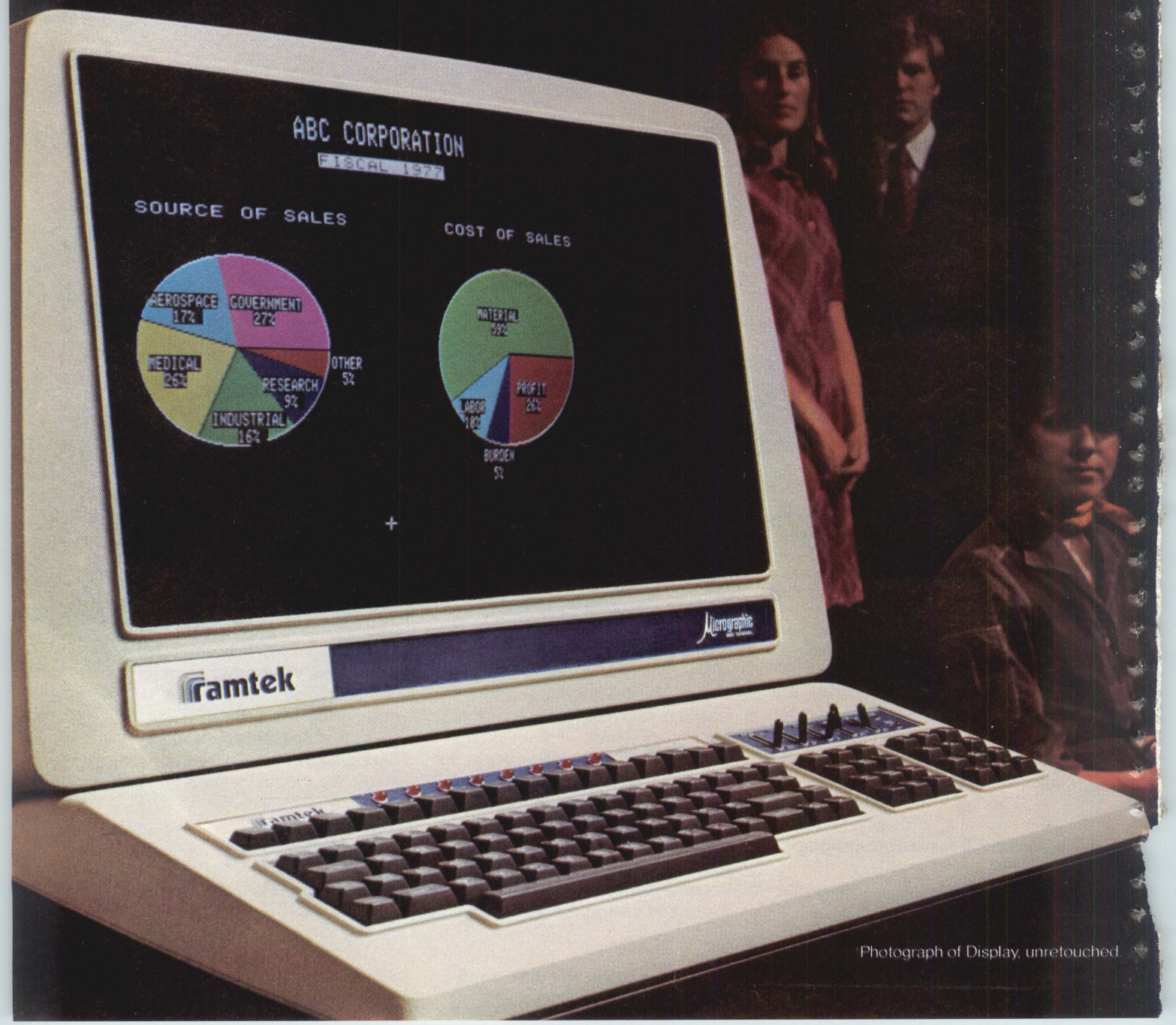
Sanders experience? Our graphic terminal systems are used in computerized production projects. Tire-tread design. Avionics defense systems. Flight training. Land-use management. Air traffic control. And dozens of other areas.

Compatible, fully equipped, low priced. What other graphic conclusion can you draw than the new Sanders Graphic 7? Send for specs and specific applications. Sanders Associates, Graphic Systems Marketing, South Nashua, NH 03060. 603-885-5280.

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CIRCLE 24 ON INQUIRY CARD

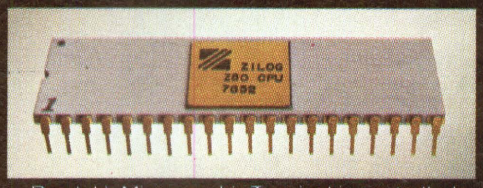
Look what Ramtek has done to graphic terminals.



Photograph of Display, unretouched

Now you can get quality resolution and a combination of true graphics and true alphanumerics at an affordable price.

Ramtek introduces the new Micrographic Terminal. No longer do you have to settle for poor resolution or give up color in economy priced display terminals. Ramtek gives you a high resolution, flicker-free display on a resolvable matrix of 512 elements by 256 lines. And you get a choice of black and white or any 8 of 64 colors as well as split or dual screen capability. The independent alphanumeric refresh offers you single character addressibility within a visible matrix of 25 rows of 80 characters that are crisp, sharp and well defined.



Ramtek's Micrographic Terminal is controlled by a powerful Zilog Z-80 with 28K bytes of PROM and 16K bytes of RAM.

In addition you can program the Ramtek Micrographic Terminal and give it the dedicated capability and intelligence you need for your application. Ramtek's software gives you TTY compatibility and high level graphic functions commanded by ASCII text strings. You can choose from an extensive list of options such as floppy disc interface, additional serial I/O ports, alphanumeric overlays, user defined fonts, color selections and packaged software.

More good news: prices for a black and white basic system begin at just $4,700 and for color at only $5,400.

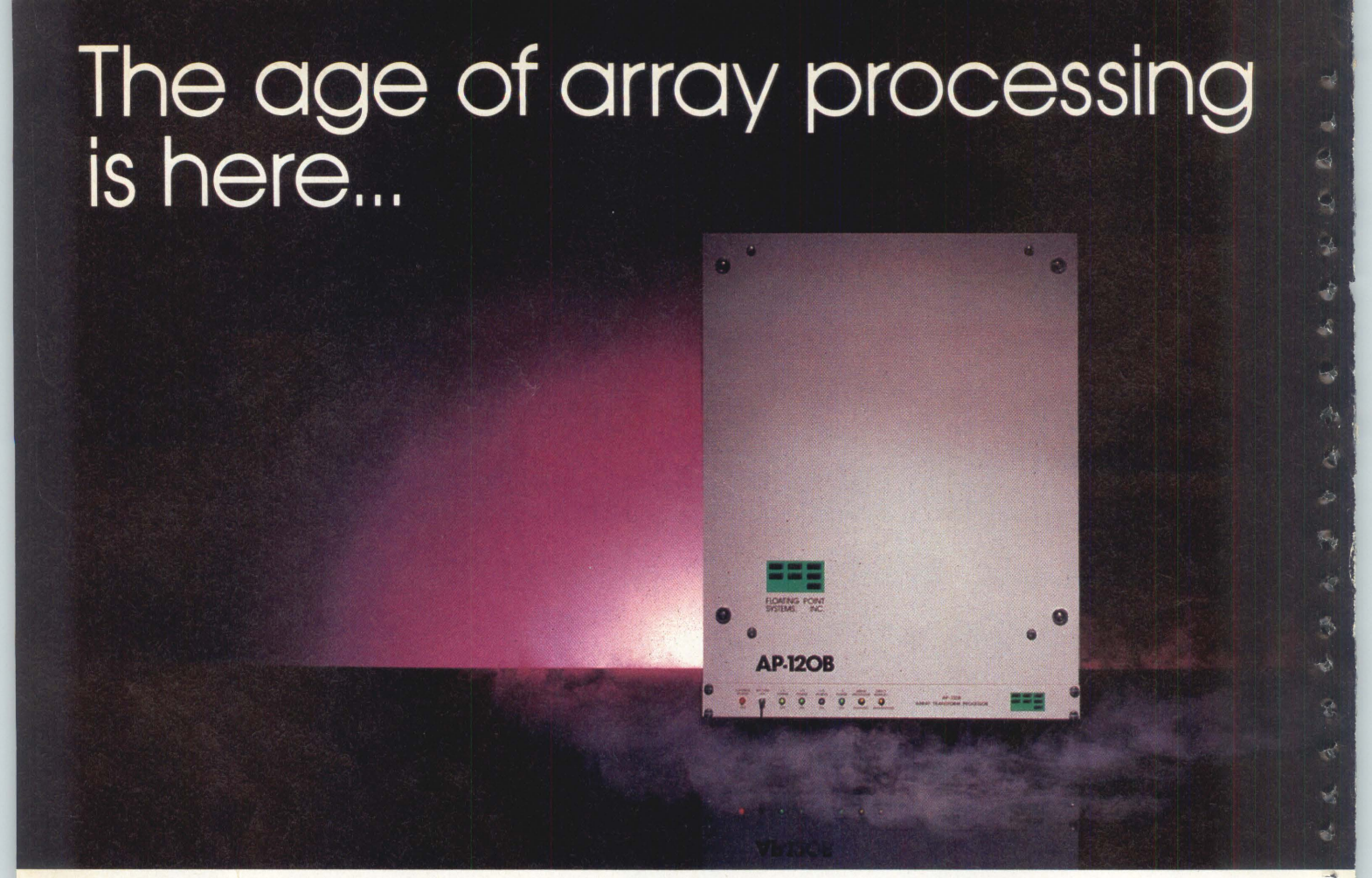
But to fully appreciate the contribution the Ramtek Micrographic Terminal can make to your application, you'll need to know more details. Just call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale CA 94806. If you're really in a hurry call us at (408) 735-8400 and ask for Todd Martin.

ramtek

Our Experience Shows

CIRCLE 25 ON INQUIRY CARD

The age of array processing is here...



THE AP-120B
FLOATING-POINT ARRAY PROCESSOR

This high-speed, programmable array processor is interfaced to most popular computer systems providing small to medium sized systems with the computational speed and power to process scientific/analysis algorithms with the enhanced throughput comparable only to large dedicated mainframes.

- SIMULATION
- IMAGE PROCESSING
- GRAPHIC RESEARCH
- METEOROLOGY
- SIGNAL PROCESSING

...and MORE

FAST: 167 nanosecond multiply/add...2.7 millisecond 1024 FFT. Throughput 100 to 200 times greater than most computers.

EASY PROGRAMMING: Over 95 routines callable from FORTRAN. Its symbolic cross-assembler and simulator/debugger helps you create new routines.

COMPATIBLE: Interfaced to all popular computers and their operating systems. A flexible format converter translates data to and from the host CPU. And a high speed DMA port is available to use with other peripherals.

CAPACITY: 167 or 333 nanosecond 38-bit memories from 8K to 1 megaword.

PRECISION: 38-bit floating-point arithmetic, **normalized and convergently rounded,** produces eight decimal digit accuracy, not just six.

RELIABLE: Goes where your CPU goes—computer room, lab, or in the field. More than two years of operation logged.

ECONOMY: A complete system less than $40K. That's a small fraction of what you must spend for comparable computing power.

Discover how the AP-120B has brought **The Age of Array Processing.** Hundreds are in use. Send for our data pack and find out what the AP-120B can do for you.

The Age of Array Processing Is Here.

FLOATING POINT SYSTEMS, INC.

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Name_____ Title_____

Company_____ Phone_____

Address_____

City_____ State_____ Zip_____

My Computer System is _____ My application is _____

See us at IFIP Congress '77
Aug. 8—12 ... Booth 140,142 ... Toronto, Canada

structures allows all data files and executable programs to be accessed for loading, modification, or execution by simple keyboard commands.

DECstation word processors consist of the WT78 word processing terminal with video display and contain the LSI processor with 16k-words memory. They manage text entry and editing in configurations ranging from standalone stations to large multiuser, shared logic networks. Using WPS-11M software, the terminals can interact with PDP-11 systems. Shared logic software makes disc storage as large as 88M bytes available to as many as 48 users, permitting entry and editing of extensive texts and simplified file management. With optional communications software, WS78 systems can interact with PDP-11 computers over telephone lines or can interact with each other.

In a standard configuration, the DECstation consists of VT78 video data processor and dual floppy disc drive; it is priced at $7895 (single quantity). A standalone WS78 consisting of WT78 terminal, dual floppy disc unit for local mass storage, and letter quality printer is priced at $13,990.

Circle 140 on Inquiry Card

Graphics Terminal Also Offers Data Entry/ Communication Features

A high performance graphics terminal, the HP 2648A combines raster scan technology and microprocessor control to provide advanced graphic features along with data entry and data communication capabilities. Among its features are an easy to read 5 x 1″ (12.7 x 25.4 cm) display on 9 x 15 dot character cells, selective erase, independent graphics and alphanumeric memories, automatic plotting of tabular data, rubber-band line, and system independent zooming and panning.

In designing the terminal, Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, used raster scan technology to give the unit a bright display even in well-lit areas. Display refresh technology also enables users to selectively erase and modify parts of the display without having to redraw the entire image. This not only minimizes the user's waiting time, but reduces CPU overhead and cuts communications costs when working in a computer network.

Separate storage areas for alphanumeric and graphic data permit separate or simultaneous display of both. For example, computer dialog can be erased from the screen to prevent interference with generated graphics. Text can be composed in graphics memory to allow the operator to label a display before transmission to a hardcopy device. Standard alphanumeric memory is 8k bytes of 4k RAM (expandable to 12k bytes). Sixteen 16k RAMs provide 360 x 720 dot resolution in the graphics display.

Zooming and panning the image is done with a single keystroke and needs no CPU support. Any segment of graphics memory can be magnified up to 16 times; users can concurrently pan any portion of the magnified display not in the viewing window without reinitializing the display area.

A rubber-band line capability allows users to stretch and then draw a line in any direction between a selected point and the cursor, speeding graphics development. Area shading and pattern generation improves architectural and mechanical part graphics.

System/software-independent automatic plotting allows a fully labeled plot to be generated from tabular data with as few as three keystrokes. The terminal guides the operator through a single menu of key questions about the data to be plotted, allowing use by those having little or no programming skills.

In addition to these graphics features, the unit offers benefits of the HP 2645A display station, which include data communication flexibility, user-defined soft keys, offline data preparation and editing capability, page and character mode operation, and built-in self test. Optional built-in cartridge tape drives provide 220k bytes of local data storage for on- or offline applications.

Base price of the 2648A is $5500; when equipped with cartridge tape drives, the unit costs $7100. Deliveries are scheduled to begin in August.

Circle 141 on Inquiry Card

Fiber Optics Used For Transfer of Data From Punched Cards

A punched card activated status board employs fiber optic transmission paths to transfer coded light signals from an information source to the visual output location—the status board. Developed at the Naval Ocean Systems Center, San Diego, CA 92152, the board eliminates human intervention in the updating process and should save considerable time and cost.

The display is made of seven optic segments; each segment, or light guide, is composed of several fibers. All numbers can be displayed through the proper combination of the seven segments. Fiber segments are brought together in a closed box and are illuminated with a high intensity light bulb. Selective masking provides control of any or all of the segments receiving light within the box. Masking is achieved by insertion of a standard prepunched card which has the desired numeric information.

Light source for each pair of read heads is three small fluorescent tubes with a total output of 21 W. Above and below each light source is a hinged door, behind which is the IBM card entry port for each fiber optics digit area.

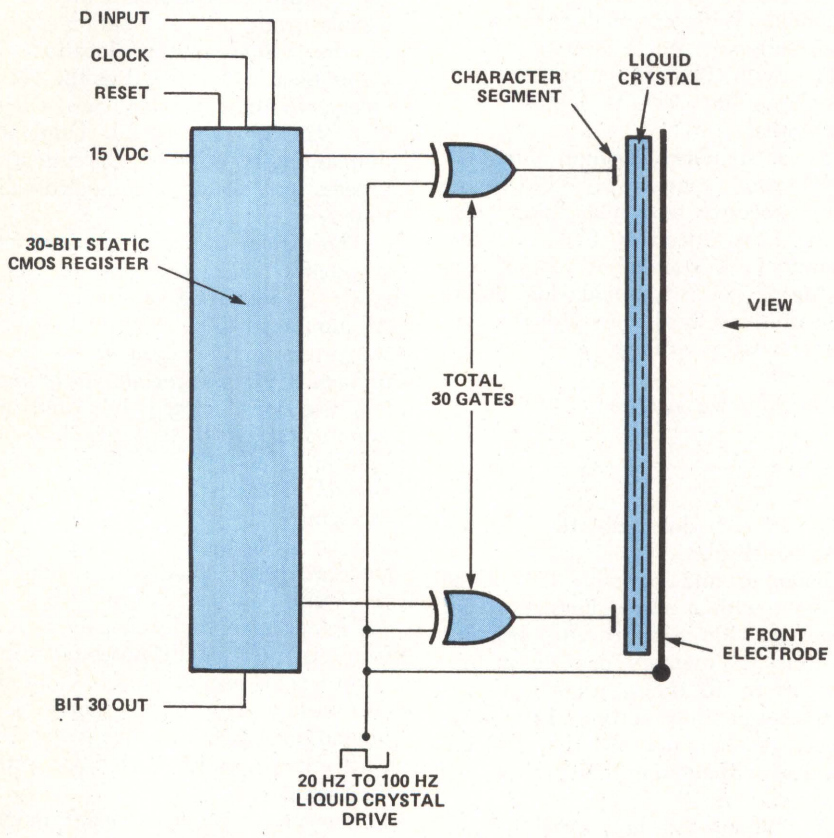
The prototype operational model, now in use to give a visual presentation of the current financial status of various projects, was built by Poly Optics, Inc of Santa Ana, Calif. The developers have been authorized to prepare a patent application covering the concept.

Circle 142 on Inquiry Card

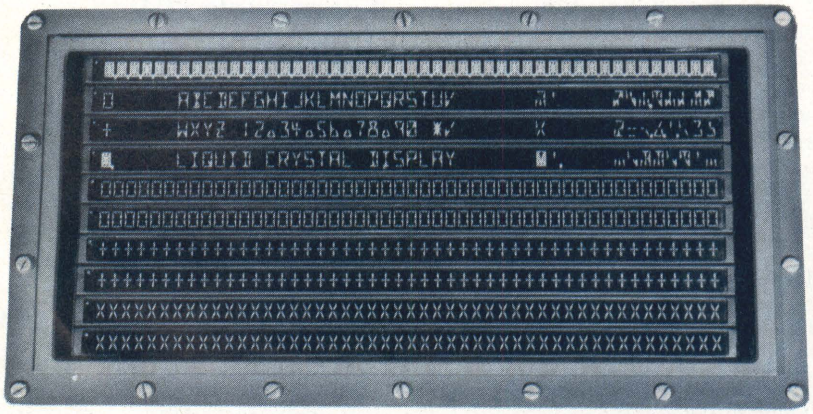
Large Scale LCD Suitable for Military Applications

An LCD with 10 lines of 48 alphanumeric characters each has been developed for military applications. Measuring 7.75 x 15″ (19.69 x 38.1 cm), the display is fully operational over large temperature extremes (−45 to 75°C) and in varying high ambient light conditions. Developed by the Applied Technology Div of Itek Corp, 645 Almanor Ave, Sunnyvale, CA 94086 under a contract from Computing Devices Co, Ottawa, Canada, the device will be used in Milipac, a ruggedized computerized field artillery fire control system.

The unit consists of 10 single-line Dyna Scat™ displays organized into



Electronic drive of the Dyna Scat LCDs is a CMOS IC which requires low power. The circuit stores last message bits until clocked or reset by a second message



Itek's large scale liquid crystal display is formed of 10 single-line 48-char displays suitable for military use. Based on dynamic scattering used in the reflective mode, the LCDs provide good readability even in high ambient light

a multiple line assembly. Each line is a replaceable subsystem, greatly enhancing maintainability. Electronics are organized with two or four characters to a submodule; submodules are mounted on the back of the LCD line.

Driver electronics consist of a custom CMOS IC. The circuit is a static serial-to-parallel shift register that stores the last message bits until clocked or reset by a second display message. Message bits are accessible at a line "data output" connection. Serial addressing provides computer compatibility. Control/timing signals consist of a serial clock and data line. Maximum clock rate is 5 MHz. All data inputs are CMOS and are positive true logic.

The unit's low power requirements —225 mW—are derived from the specially developed CMOS circuit. The circuit provides the ac drive to the liquid crystal material and also reduces the number of wires required to connect the display to the external drive circuitry.

Dense 4-char/in character arrangement is made possible by a pins-in-glass technique which routes contacts through the backplate rather than conventionally to the edge. An electrode pin connection is provided for each liquid crystal character segment. The electrode pin is molded in the glass plate. In addition, service lines for the electronics and heater wires are fully encapsulated in the glass backplate. The technique allows dense electrode spacing (up to 30/in—12/cm) and reduces outside wiring to the absolute minimum.

Based on dynamic scattering used in the reflective mode, the LCD's reflective nature makes it extremely readable in high ambient light. Average contrast ratios as measured with a photo research spot photometer and diffuse background lighting are 20:1 or better. The material is normally clear in the unexcited state, and light incident to the display is reflected from the mirror back surface to a light trap or black hood. When energized, the liquid crystal becomes turbulent and scatters light to the eye, creating an image.

Circle 143 on Inquiry Card

Optical Video Disc System Offers Fast Retrieval of Color Still Pictures

A large capacity, optical video disc system for storage and retrieval of color still pictures by means of laser


The system builder's sensible display.
Everything you need and not one piece more.
Tektronix

We've combined refresh with storage in a new modular graphics display.

You build from there.

Suddenly state-of-the-art display technology comes built for the OEM.
Tektronix' new GMA display modules let you integrate into your system our most impressive display capabilities ever. Including refresh and storage graphics in one tube. Complete character and vector generators. Big 19″ screen and fine resolution.

It's exactly what you need, because you can specify exactly what you want. Order CRT and power supply only, or select from a range of performance and packaging options in our extensive product line.

You can integrate other products from our graphics family, like hard copy modules. Or talk to us about other special product configurations, like our 11″ storage-only components.

No other package lets you pick such comprehensive graphic display capability at anywhere near the price.
It figures, because Tektronix has been the worldwide low-cost graphics leader for years. No matter what unique and unusual systems you're working with, we can help with manufacturing flexibility, engineeering assistance, and a passion for excellence.

Get capability you can build with. From a supplier you can work with. Get your Tektronix OEM Sales Engineer on the phone today. Or write us for more information.

Tektronix, Inc.
Information Display Group
OEM Components
P.O. Box 500
Beaverton, OR 97077

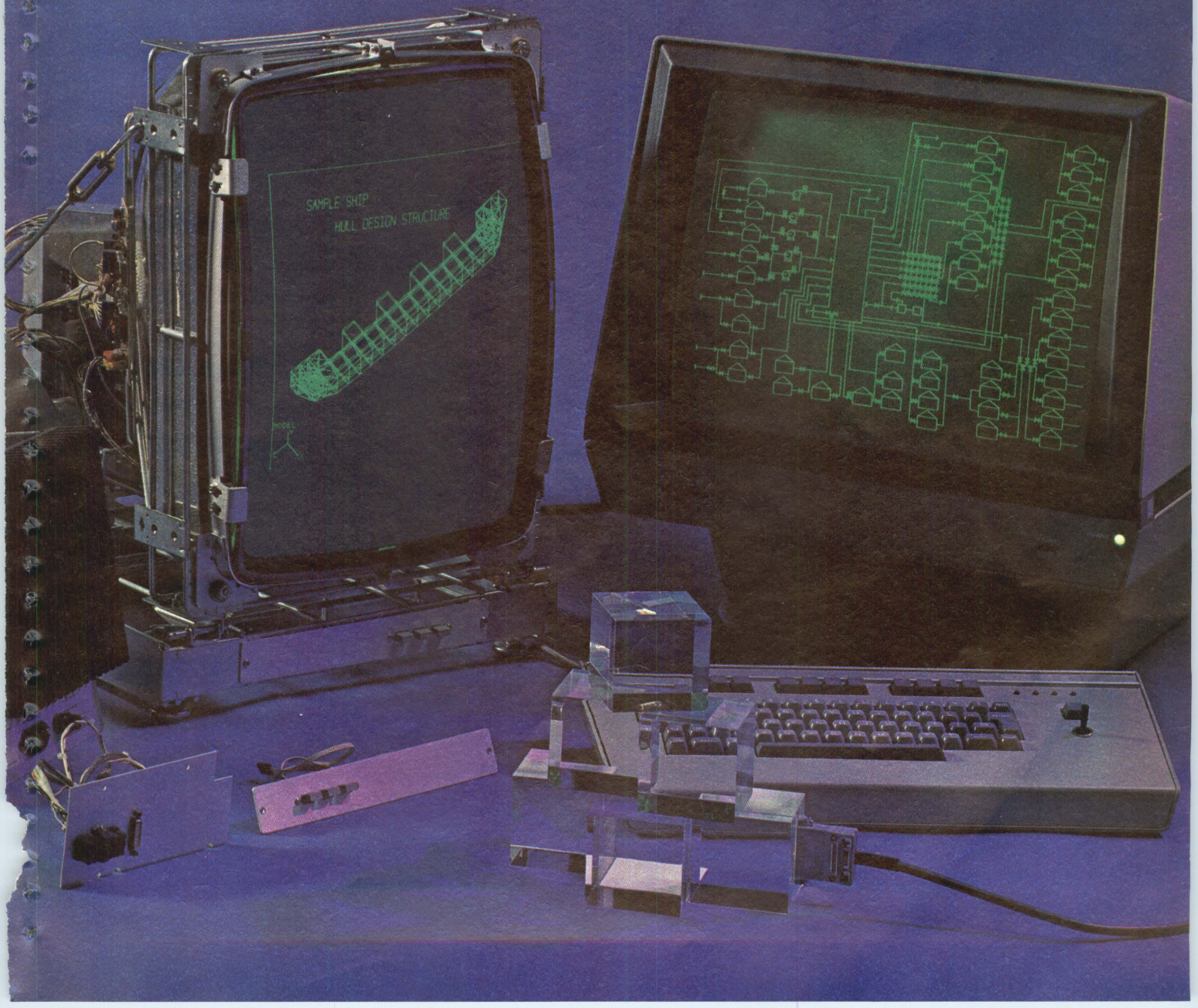
CIRCLE 27 ON INQUIRY CARD



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Tektronix OEM components: the perfect fit.

Tektronix®
COMMITTED TO EXCELLENCE



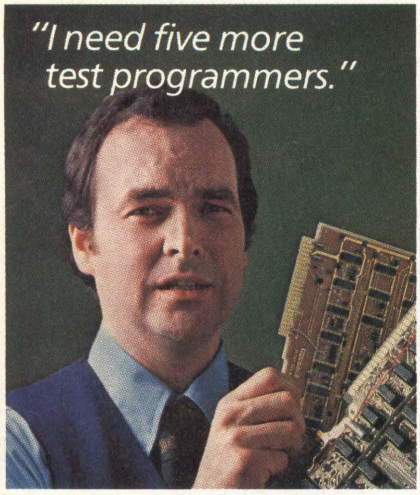
The P400 makes excuses obsolete.

A new product comes on line and the circuit boards start piling up. This is when the excuses begin:

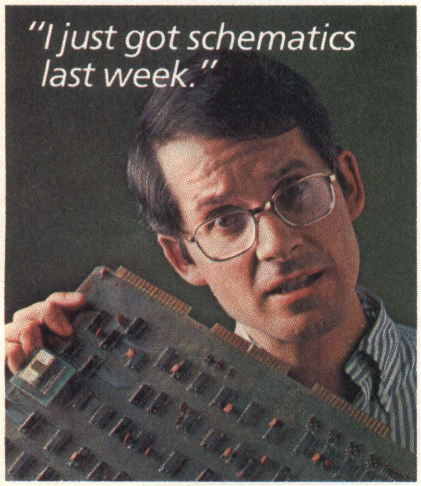
"I can't get near the computer."

"I need more programmers."

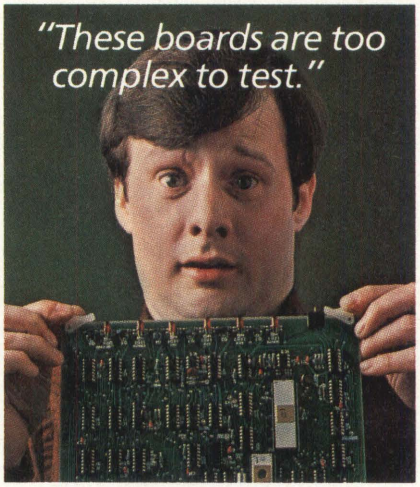
"I just got schematics last week."



It's a difficult time for a test engineer because the success of an important product can hang in the balance.



But Teradyne's P400 Automatic Programming System has changed all that. Used with L100 series test systems, the P400 creates the entire test program



automatically. It gives you all input patterns, provides all diagnostic data, and resolves all races. It cuts programming time from weeks to days. And it does it all without tying up the computer on your production tester or increasing your programming staff.

Suddenly, new programs can be ready on time, even in the face of the tightest schedules. And even for the most complex boards.

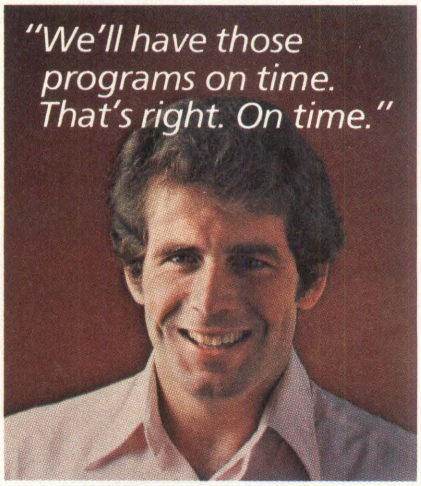
Just as important, the P400 spares you all the boring work it usually takes to deliver new programs. You get typically better than 95% fault coverage simply by using the telephone to access a large computer containing the P400 software.



The P400 Automatic Programming System.

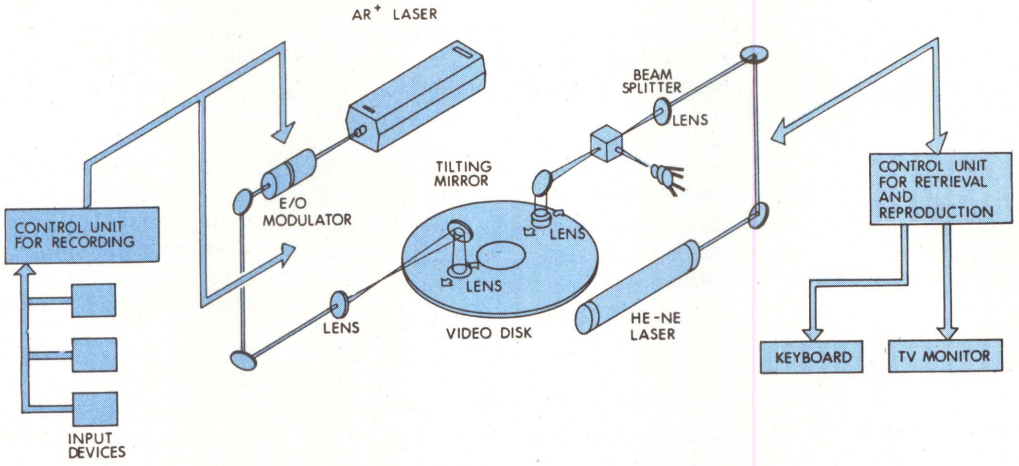
Now there's no reason for being late.

And we think that's the way you want it.



TERADYNE

183 Essex Street, Boston, Mass. 02111



Optical video disc system records and retrieves data using a laser, eliminating the need for processing and fixing. Hitachi's prototype system uses computer circuits for high speed random access to information. It can record 50,000 to 100,000 signatures on one disc and retrieve them within 0.5 to 3.0 s

technology has been developed by the Central Research Laboratory, Hitachi, Ltd, New Marunouchi Bldg, No. 5-1, 1-Chome, Marunouchi, Chiyoda-ku, Tokyo, Japan. The prototype system can record 50,000 to 100,000 signatures on one 30-cm diameter video disc, and is capable of reproduction and retrieval in 0.5 to 3.0 s.

Picture information, transmitted through a television camera or VTR, is recorded by means of a laser beam 0.6 μm in diameter, on a video disc 30 cm in diameter turning at 30 rev/s. A glass sheet plated with a thin metal film is used; because a laser is used, no processing or fixing is required.

For reproduction, a 1.0-μm diameter laser beam is directed at the track of the revolving video disc, and its reflections are read and converted to picture form on the color television tube. The prototype system employs computer circuits for high speed random access to information on recording and reproduction control units.

Reproduction of the desired picture is accomplished through keyboard pushbutton operation. In the retrieval process addresses are encoded and recorded simultaneously with the picture on the track.

The reproduced picture is comparable to high quality color television reproduction, with signal-to-noise ratio of more than 40 dB. With large storage capacity and the capability for quick retrieval of image information, the system can be applied in such areas as for depositors' signatures in banks, or for X-ray photographs in hospitals, and is expected to find application in visual communications where coordination with a facsimile is required.

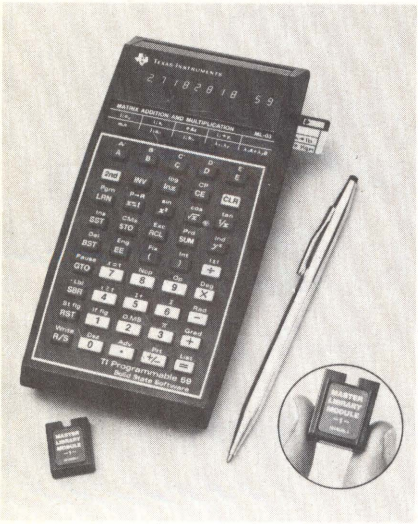
Circle 144 on Inquiry Card

Plug-In Modules Enhance Memory Capacity of Programmable Calculators

Using plug-in interchangeable solid-state modules that contain up to 5000 program steps each, the Programmable 58 and the Card Programmable 59 calculators, from Texas Instruments Inc, Calculator Products Div, PO Box 5012, Dallas, TX 75222, offer significant additional program memory capability and programming flexibility. With the PC-100A printer, which provides alphabetic character printing and plotting capabilities, the calculators become desktop machines.

Solid-state software modules contain prerecorded programs. The library ranges from applied statistics and surveying to real estate/investment, aviation, and marine navigation. Programs in the module can be addressed repeatedly from the calculator keyboard or can be inserted as subroutines in other programs developed by the user. Contents of the module cannot be altered, although users of the model 59 may record up to 960 steps of any program on two magnetic cards. Program data and listings can be printed by the print unit.

Other than the magnetic card memory capability of the Programmable 59, which allows 960 program steps to be recorded on two magnetic cards for storage and loading into the calculator, the calculators differ only in storage capacity. Users can partition the 58 with up to 480 program steps or up to 60 memory registers; the 59 can have up to 960 steps or up to 100 memory registers. For every increase or decrease by 10 memories, 80 program steps are added or taken away in storage. Changing



Plug-in prerecorded ROM modules containing program libraries offer significant amounts of additional program memory capability and programming flexibility to Texas Instruments' Programmable 59 calculator. Interchangeable modules contain up to 5000 program steps each

program steps affects the amount of memory in the opposite way. With the 59, however, when all 100 memory registers are used, 160 program steps remain available.

Both units have up to 10 registers available for looping, increment, and decrement, and the same number of user flags for set, reset, and test. Up to six levels of subroutines are available along with four types of display testing with an independent test register. Absolute, indirect, and label modes are provided for addressing program steps; data registers can be addressed in direct or indirect modes.

An algebraic operating system (AOS) allows complex equations to be entered the way that they are algebraically stated, from left to right. The system enables the calculator to execute problems automatically according to the rules of algebra.

Available for use with both units, the PC-100A printer offers alphabetic and special character printing and plotting capabilities. The unit provides 64 characters including blank spaces on 2.5" (6.3-cm) wide thermal paper; maximum line length is 20 characters. Printing speed is more than three lines or 60 char/s. Plot curves or histograms can be made from the calculator keyboard or directly from a program. A listing format shows key symbols and codes as well as the contents of all memory registers and all program labels and their location.

Prices for the devices are model 58, $124.95; 59, $299.95; PC-100A, $199.95. Software modules have a price of $35 each. Both calculators come with instruction manual, a master library Solid State Software module, and manual covering 25 prewritten programs in mathematics, statistics, and other application areas.

Circle 145 on Inquiry Card

Low Cost Business Computer Systems Based on COBOL

COBOL-based Commercial Systems CS/40 series support up to nine interactive data entry and display stations, allowing the implementation of business functions with familiar techniques. Announced by Data General Corp, Westboro, MA 01581, the systems are designed for transaction driven applications, where data are processed immediately upon entry. They combine interactive ANSI 74 COBOL and utilities with a sophisticated operating system and operator-oriented hardware for ease of implementation and use in various applications.

Systems can be operated by existing personnel and can be programmed by COBOL programmers without special minicomputer training. COBOL file management facility allows easy creation of interactive displays such as menus from which the operator can select appropriate data entry and display functions. "Fill-in-the-blanks" screen formats simplify data entry and access.

File management features provide comprehensive direct file access by all stations on a timely basis. Systems can support sequential, relative, and indexed sequential (ISAM) files. A file and record locking feature assures orderly concurrent access to files, by preventing more than one operator from accessing the same record simultaneously.

Systems can support synchronous communications with other family members, larger Data General host systems, or IBM-compatible host installations. Batch communications are controlled via the RJE 80 facility using 3780/2780 protocols.

The family consists of three models: Mod C1 supports one CRT station and includes a 10M-byte cartridge disc subsystem, 64k-byte processor, and choice of 60-char/s terminal printer, 165 char/s serial printer, or 300 line/min line printer; C3 systems support one to four CRT stations; and C5 systems support one to nine CRT stations. Simplified expansion procedures let users add terminals and disc capacity up to 40M bytes. Magnetic tape and diskette capabilities can be added as well.

Representative prices for the systems including COBOL language and system utilities are: C3 with three Dasher display terminals, 64k bytes of MOS memory, 10M-byte cartridge disc subsystem, single diskette drive, 60 char/s Dasher terminal printer, three work station disks, and single bay cabinet; $40,245; a C1 system with one terminal and workstation desk, all other equipment the same, is priced at $33,415. A C5 with five display terminals, 128k-bytes memory, 20M-byte cartridge disc, magnetic tape subsystem, 300-line/min printer, and synchronous communications option will cost $82,100. First shipments are scheduled to begin in September.

Circle 146 on Inquiry Card

Dual-Port Disc Controller Enables Breakdown Immune Data Access

An intelligent, microprocessor-driven disc controller and 200M-byte 3330-type disc drive expand the ability of T/16 NonStop™ computers, from Tandem Computers Inc, 20605 Valley Green Dr, Cupertino, CA 95014, to provide cost-effective transaction processing and modular expansion. T16/3103, a dual-port disc controller, interfaces up to eight 200M-byte drives to the computer system to offer increased processor efficiency, flexible disc storage configuration, and breakdown immune data access. The T16/4103 disc drive has an 806k-byte/s transfer rate with average access time of 30 ns and average latency of 8.3 ns.

Featuring a 4k-byte block buffer that improves processing efficiency by reducing interprocessor data transfer and I/O channel transmission, the controller provides a read-without-transfer capability that allows data to be copied onto mirror volumes or separate disc drives, without using an I/O channel. Using this capability,



THE ONE MICROCOMPUTER THAT TACKLES EVERY JOB

Product Development • Micro Control • Data Processing

UNIVERSAL 8080 AND 6800 SYSTEM $3,850

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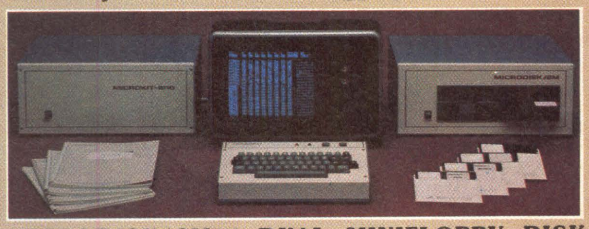
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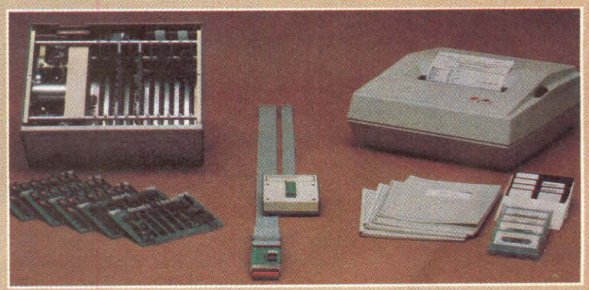
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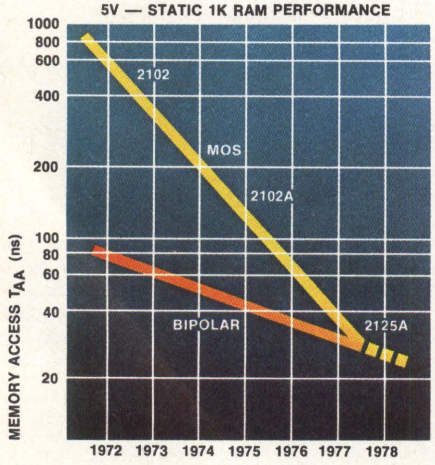
Intel delivers MOS RAM's

Convert to the Intel® 2115A and 2125A and enjoy MOS economy, bipolar speed and power savings up to 50%. These new NMOS RAMs offer 45 nsec worst case access time and a 100 quantity price of only $6.90. And that's just the beginning of the cost/performance advantages you can expect from Intel's new +5 volt, silicon gate static MOS RAMs.

The new 2115A and 2125A RAMs are pin for pin, plug-in replacements for the popular 93415 and 93425 bipolar RAMs. They offer all the same advantages. No need for external clocks or refresh circuits, fully TTL compatible, 16mA output sink current and operation from a single +5 volt supply.



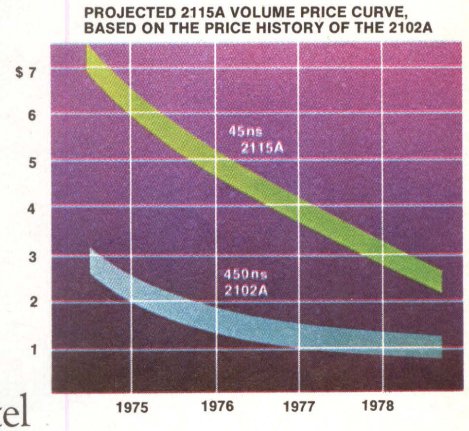
In addition, the 2115A/2125A dissipate 20% less power and the 2115AL/2125AL 50% less power than the 93415/93425. This saves power supply and cooling costs which all adds up to additional savings in the cost of your system. And there's more. Unlike bipolar RAMs, the 2115A/2125A use only a single layer of metalization which means lower manufacturing cost and a more reliable process. So you can look for continued improvement in cost/performance. To put the cost potential in proper perspective, consider this: The 2115A/2125A chip is 35% smaller than Intel's industry standard 2102A. And the



to match bipolar speeds.



2115A/2125A are made on the same manufacturing line and with a process similar to the 2102A. If you've been following the 2102A price curve you'll understand the significance.



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For your copy of our new 2115A/2125A brochure, write: Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051. In Europe, contact Intel International Corp. S.A., Rue du Moulin à Papier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814. In Japan, contact Intel Japan Corporation, Flower Hill-Shinmachi East Bldg. 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154.

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✻ Our quantity-50 OEM price for the *Silent 700*† Model 743 KSR Terminal is now just $1088. In larger quantities, the price goes below $1000.

And it keeps on costing less because the real payoff is in the cost of ownership. In the long run, it costs less than any other printer terminal with comparable performance.

The reason is easy. Superior design. The 743 KSR is built around a TI microprocessor. So, there are fewer components and circuit boards than in other printer terminals. That means less maintenance and more uptime performance. Plus standard EIA and current loop interfaces in a lighter, desk-top package.

The 743 features the speed, reliability and quietness that made the *Silent 700* terminal family so popular. Incoming data is buffered, so you get true 30-character-per-second throughput.

TI's Model 743 KSR

Disturbing noises associated with impact printers are eliminated with the 743's non-impact electronic printing.

Use it as a console I/O for software development. Keyboard terminal for inquiry/response.

Data entry. Interactive remote computing. Or as a message terminal network. And it's now available with APL. The 743 is backed by TI's worldwide maintenance and support services.

Find out more about TI's 743 KSR printer terminal. Fill out and mail the coupon today. Or call your nearest TI sales office, or Terminal Marketing, (713) 494-5115, extension 2126.

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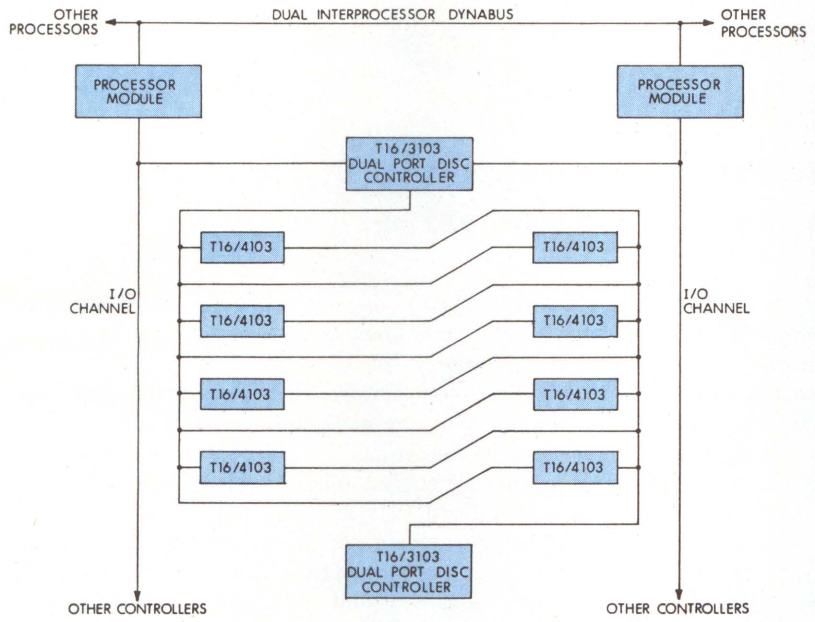
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*U.S. Domestic Price

TEXAS INSTRUMENTS.



A microprocessor-driven dual port disc controller, Tandem Computer's T16/3103 interfaces up to eight 200M-byte disc drives to NonStop systems. A 4k-byte block buffer in the unit improves efficiency by reducing interprocessor data transfer and I/O channel transmission

the primary processor merely sends a checkpoint to its backup when the controller has accepted the data block, and then transfers data from the controller to the disc units. The result is a substantial increase in processing efficiency and in breakdown immunity.

By using the data buffer for fast copying of one data volume to its mirror, the controller enhances capability of the data base record manager. It performs error correction in the buffer on data read from disc, before data are transferred. Data overrun problems encountered in subsystem channels are eliminated, since an entire data block is held in the controller buffer for transfer to disc. Up to 32 disc transfers may progress simultaneously.

The 200M-byte disc drive features dual accessibility by disc controllers. Two ports allow it to attach to two disc controllers simultaneously; if one goes down, the other can maintain access to the data base.

Circle 147 on Inquiry Card

Computers Based On Migration Path Concept Offer Choice of Mode

Providing users with a choice of operating modes, three computer systems are based on the "Migration Path Engineering" concept. Announced by NCR Corp, Dayton, OH 45479, the -8350, -8450, and -8560 allow users to choose to operate as a Century system (N-mode), as a virtual storage system (V-mode), or in interactive systems mode (I-mode) with the required performance level. All systems are designed to operate within a complete communication architecture to be ready this summer.

The general-purpose N-8350 has a processor cycle time of 1.2 μs and minimum memory size of 32k, expandable to 128k. It is a disc-based system featuring cassette I/O and a CRT console for visual control.

Using a multiple-mode processor derived from Criterion-type architecture, the N-8450 offers an upward migration path for current Century users; with the same basic processor, the medium sized V-8450 provides the benefits of operating in a virtual storage mode. These machines have a standard processor cycle time of 112 ns and minimum memory sizes of 128k (N) and 384k (V). Memory is expandable in 64k increments to the 1M-byte maximum. An I-mode version is planned for introduction later this year.

Most powerful of the computers, the V-8560 employs Criterion architecture and the Virtual Resources Executive (VRX) operating system. The unit features 84-ns processor cycle time, emitter-coupled logic, from 384k to 1.5M bytes of main memory, and up to five I/O trunks. The N-8560 system for non-VRX applications has a minimum of 192k bytes of main memory.

By emphasizing applications development and turnkey programs that can be customized to special user requirements, the total system philosophy provides a hedge against rising costs. A large library of existing applications software allows many programming, testing, and documentation costs to be avoided. High degree of system compatibility controls the nonhardware costs that rise dramatically as requirements grow, reducing or eliminating future conversion costs.

With customer deliveries scheduled to begin from July through the end of the year, representative prices include $69,650 for an N-8350 with 32k memory, 10M-byte disc storage, and 150-line/min printer. A virtual-mode -8450 processor with 384k memory sells for $142,250, and a V-8560 with 384k memory has a purchase price of $237,050.

Circle 148 on Inquiry Card

Refurbished Disc Heads Hold 1-Yr Warranty

Disc heads from all major manufacturers can be repaired and refurbished using a service provided by the Infoextend group of Information Magnetics Corp, 5740 Thornwood Dr, Galeta, CA 93017. Refurbished products have the same 1-yr warranty offered with new heads.

All inspection, mechanical measurements, and dynamic electrical tests are done on equipment identical to that used in building new heads. Load force, attitude, gap alignment, microscopic visual inspections, and electrical characteristic measurements are made on equipment that is calibrated and correlated to industry standards. □

Circle 149 on Inquiry Card

Efficiency of Electric Power Generation and Distribution Improved by Energy Management System

Even before energy crises became routine subjects of conversation and discussion for politicians, homeowners, industrialists, and just about everyone else, most electric utilities were seriously attempting to increase the operational efficiency of their power stations. Success in any of these attempts improved customer service and, not incidentally, increased profits for the utilities.

Dominant problems that led to failure in meeting customers' demands were insufficient generating capacities and inadequate distribution systems. The target for the utilities, therefore, was to provide sufficient power at all times, with backup to meet fluctuating demands, over effectual transmission lines—but to do so at the lowest possible operating cost.

Although no system will be foolproof so that there will never be loss of power to customers during major storms or similar near disasters, an efficient system should contain ways of remedying malfunctions rapidly. A beginning towards meeting these goals is a supervisory control and data acquisition system that will provide dispatchers with sufficient information about their power generating systems to permit them to make decisions quickly.

One such scheme is the standard energy management system (SEMS) designed by Moore Systems, Inc, 1212 Bordeaux Dr, Sunnyvale, CA 94806. All SEMS installations are fundamentally the same. They control power output of generators and power flow to match supply with demand, maintain backup, locate and sometimes control malfunctions, and monitor and report on operation. However, each has unique features that meet particular requirements of its installation.

Basic SEMS Configuration

Primary requisite for an effective energy management system is the ability to collect up-to-date data, communicate with a central master station, and present the data clearly such that operators can make rapid, accurate decisions. In addition, it must be able to control power system elements efficiently from the same central station.

As a minimum, an energy management system requires full implementation of supervisory control and data acquisition disciplines. Some system requisites are device control, status monitoring, alarm detection and reporting, event logging and report generation, dispatcher and programmer functions, and automatic fault detection and failover (recovery of failed subsystem by redundant circuit). Optionally, the system can also contain automatic generation control (AGC).

SEMS achieves operational continuity through full redundancy: redundant computers, redundant bulk memory, individual peripheral controllers for each CPU, and dual-ported peripherals. A system integrity monitor (SIM) provides automatic failover to the backup system in case of malfunction.

Each master station (see Fig 1) comprises two Digital Equipment Corp PDP-11 computers, each equipped with memory management hardware, extended instruction set, power fail/restart, real-time clock, multiple levels of interrupts, and sufficient core and disc storage for the application. Each CPU has its own totally independent bus and interface for every device. Individual peripheral devices are connected to the interfaces through failover switches which allow access by either CPU.

This "dual porting" of peripherals assures that no single failure will cause loss of a system function. SIM constantly monitors operational integrity of the two computers. It allows them to perform independent operation, yet is always ready to switch control if any malfunction occurs. Either CPU can be the online processor, but if that processor fails, SIM switches the backup processor online and reverses assignment of peripherals. This change in system status is indicated to the operator on the SIM control panel

A manual override switch permits the operator to assume absolute control of the system if SIM should fail. In addition, pushbuttons are provided to allow any peripheral to be individually switched to the standby processor for maintenance or diagnostic purposes without affecting system operation.

Man-machine interface is enabled through an Aydin Controls 7-color graphics display generator, one or more 19″ (48-cm) color CRT displays, alphanumeric keyboard, and logging devices. A single display generator can handle up to four display positions, each with its own refresh memory and keyboard. System data are presented to the operator in both tabular and schematic formats, with dispatcher information in conversational (English) mode.

Logging devices are Digital Equipment Corp LA35s. A typical configuration might include a logger for each operating position for alarm and event copy plus one or more for logging periodic data.

Remote stations, Moore Systems MPS 9000 series, communicate with the online computer over 4-wire channels via 1200-baud data sets. Each of these stations is built with functional logic cards that plug into printed circuit board backplanes, and contains a multiplex unit

New Hytype Terminal for OEM's!

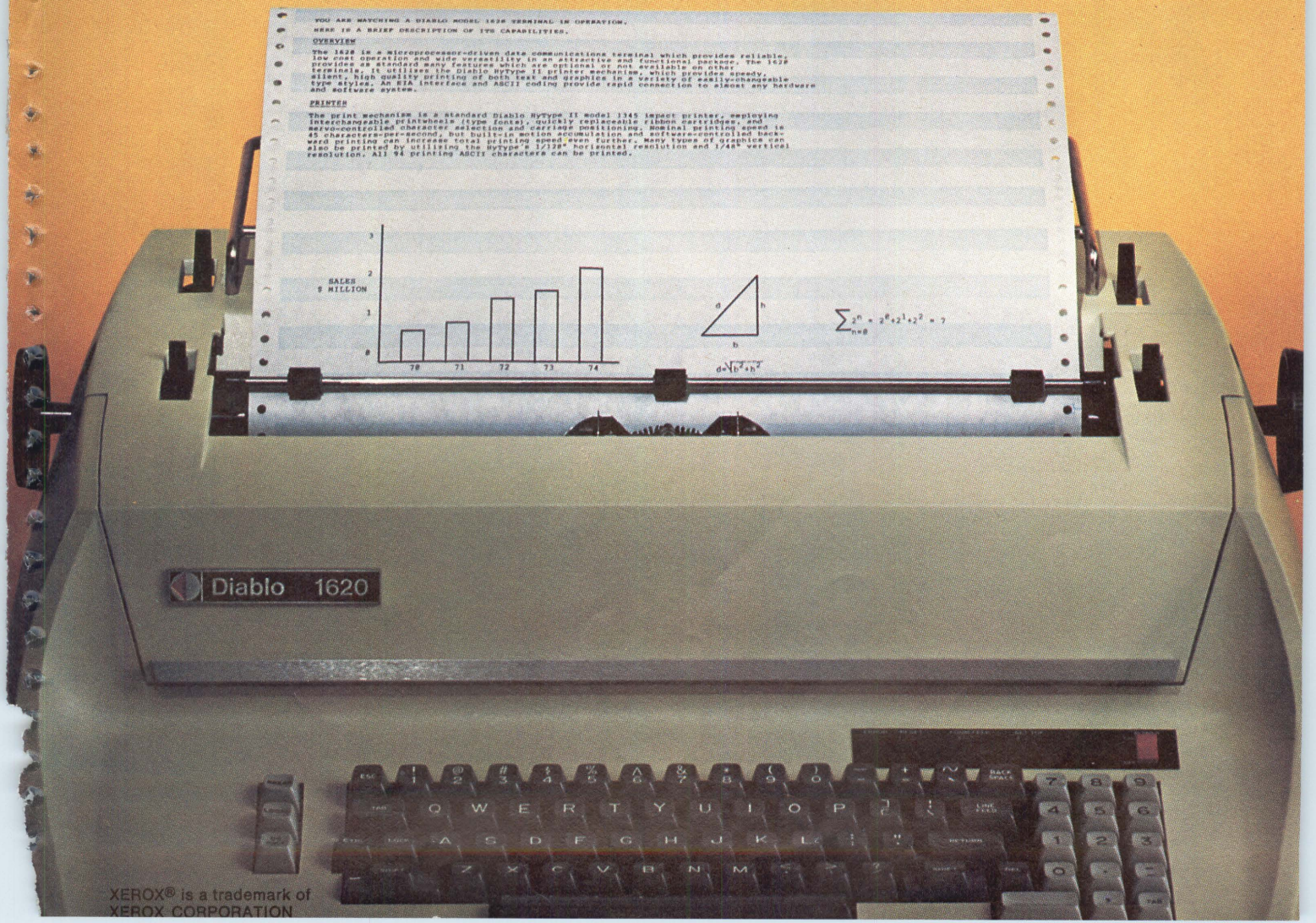
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We call it HyTerm and we've given it all the proven HyType reliability and maintenance ease. HyTerm is controlled by a microprocessor for speed, efficiency and versatility. It utilizes the new Diablo HyType II Printer mechanism noted for its typewriter print quality and speed. HyTerm is interface compatible to RS-232C and communicates in standard ASCII code. Both Receive Only (RO) and Send/Receive (KSR) models are available. All logic and circuitry, microprocessor, memory, and power supply are contained within the cover. Printer flexibility is maintained so software can initiate the mechanism's unique graphics performance, and its inherent high-speed horizontal and vertical tabbing and backwards printing capabilities. Other features: control panel and switches, audible alarm, variable format control, escape-code functions, full ASCII character set, keyboard overflow buffer, 158 character print buffer, and data error detection. Numeric pad, pin feed platen, and form tractor feed options are available. For complete specifications and features, write Diablo Systems, Inc., 24500 Industrial Blvd., Hayward, California 94545, or Diablo Systems, S.A., Avenue de Fre 263, 1180 Brussels, Belgium.

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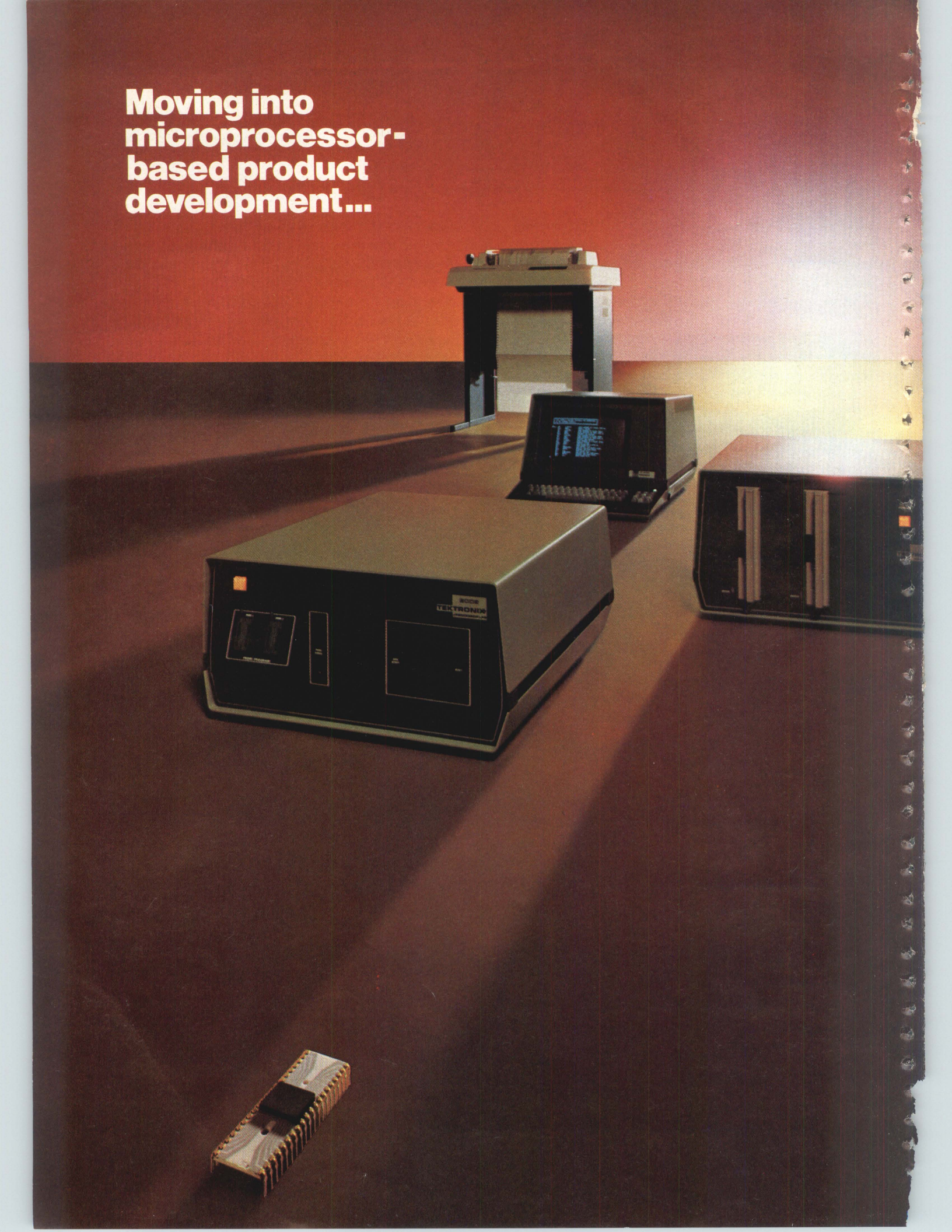
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Moving into microprocessor-based product development...



doesn't have to be a costly, time-consuming business.

Now Tektronix introduces the 8002 Microprocessor Lab, to help you meet your project deadlines and save on some of the spending.

Featuring an innovative multiple-processor architecture, the 8002 software development system supports a variety of microprocessors: at introduction, the 8080 and the 6800; next the Z-80 (available late summer 1977); then an expanding selection. Assembler software for two components is provided from those available at the time of purchase, and software for each additional microprocessor may be added optionally with a minimum of added expense.

Follow Your Own Direction

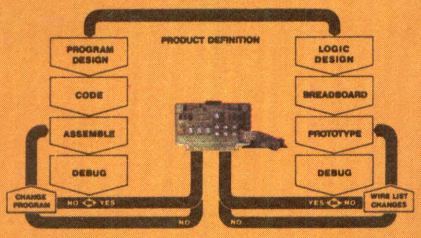
Now it is no longer necessary to buy a new microprocessor development aid each time you decide to use a different microprocessor chip. You and your team don't need to go through a new learning cycle with your equipment each time, either.

The 8002 can also save you time with several features that ease the task of program creation: a text editor that simplifies software entry and revisions, an assembler with macro capability, and dynamic trace for software debugging.

Integrate As You Go Along

Since microprocessor-based program creation and prototype design typically go hand in hand, the 8002 offers three progressive option levels for program emulation and debugging, prototype emulation and debugging, and real-time prototype analysis.

The 8002 Program Emulation and Debugging System, which adds an emulator processor and software for a selected microprocessor, enables the developmental software to be run, tested, changed, traced, and debugged on the desired microprocessor. The emulator microprocessor is identical to the microprocessor in the designer's



prototype; if the software is to be executed on an 8080 in the prototype, for example, an 8080 micropressor chip is used in the emulator processor.

The 8002 Interactive Prototype Emulation and Debugging System adds a Prototype Control Probe for a selected microprocessor. With the probe inserted into the prototype, developmental software and hardware may be tested, traced, and debugged together.

The 8002 Real-Time Prototype Analyzer System adds real-time trace and an 8-channel Analyzer Probe. At this level bus transactions and events external to the microprocessor may both be monitored.

From the Instrument Company

One final advantage: the Tektronix name. Tektronix has always been responsive to the instrumentation needs of the design engineer . . . and the 8002 Microprocessor Lab is no exception. Its ability to deal with a number of different microprocessors, its many convenience features for software development, and its capabilities for software/hardware debugging, make it a unique design tool.

As a leading electronics instrument company, Tektronix offers you a full line of options and peripherals, from the three 8002 option levels . . . to PROM programming facilities for the 1702 or the 2704/2708 MOS PROMs . . . to a line printer and choice of system terminals.

Backed by years of experience, Tektronix also offers you a rare commodity in the field of microprocessor development tools: local Field Engineers and local service. A nation-wide network of Field Offices and Service Centers is ready to help you realize the full benefits of the 8002.

For more information or a demonstration of this new software development tool, write Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077.

For availability outside the U.S., please contact the nearest Tektronix Field Office, Distributor, or Representative.

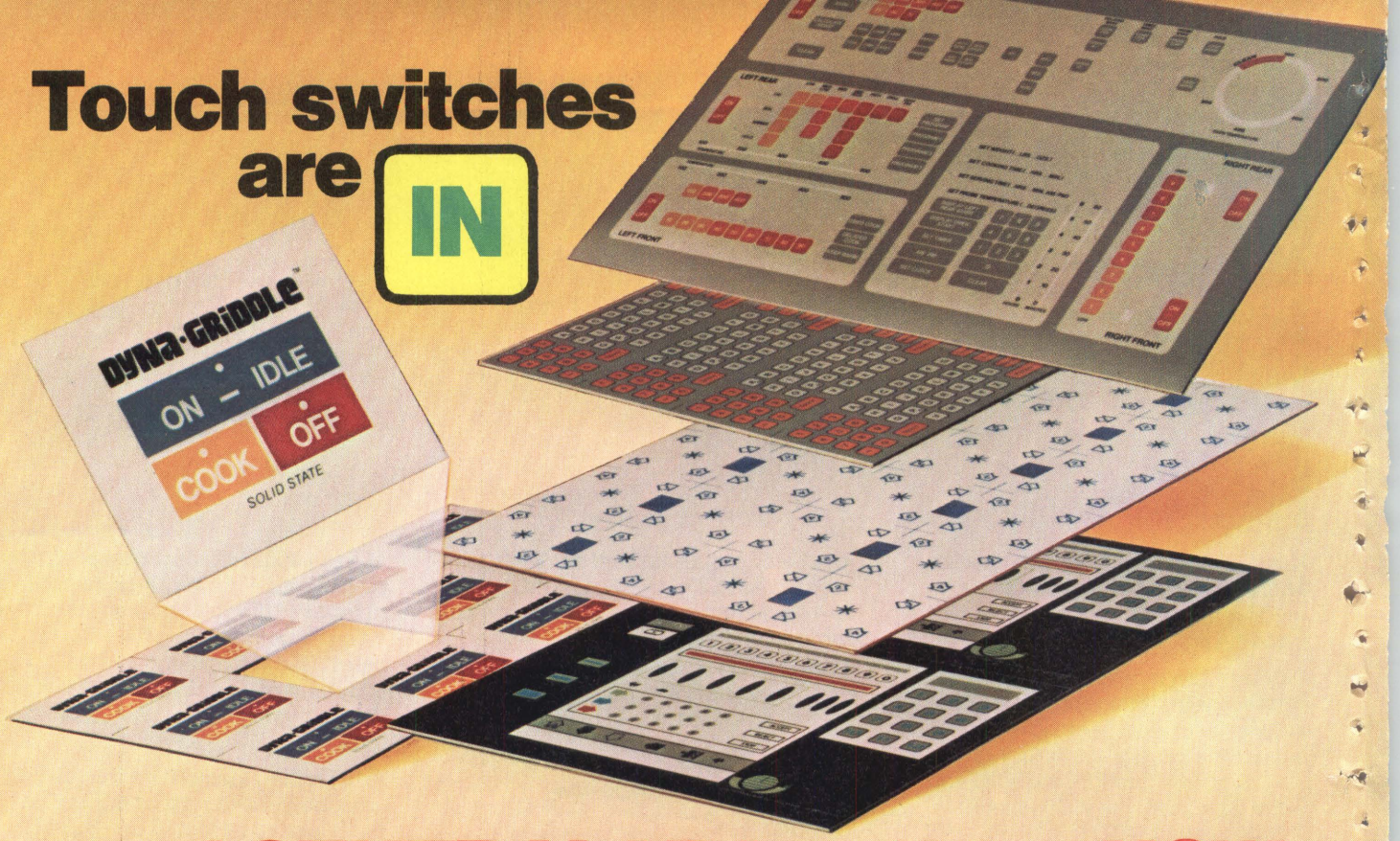
The 8002... with multiple microprocessor support.



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For a demonstration, circle 33 on Inquiry Card.

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...and CENTRALAB has them NOW

When Centralab introduces touch switches you can be sure they're "In". Backed by 40 years of switch know-how, and after years of intensive research and testing, Centralab is now delivering, in batch-process volume, a complete touch switch system. We call it MONOPANEL.

MONOPANEL is a thin, light, flat, front panel subassembly containing micro-motion touch switches already mounted and interconnected . . . with LED's, nomenclature, graphics and colors to meet your functional and aesthetic requirements.

Batch-Processed For Economy With Quality

MONOPANELS are batch-processed as 11″ X 17″ master panels only .075″ thick, each containing up to 700 switches. Every Monopanel is a complete, 100% pre-tested subassembly containing switches, front panel and graphics.

60,000,000 Cycles Without Failure!

The basic MONOPANEL switch has been operated for sixty million switching cycles without mechanical or electrical failure. And MONOPANEL has been tested and proven against 22 separate mechanical, electrical and environmental standards.

Custom Designed For Your Application

On each 11″ X 17″ panel you can custom-design individual boards to meet your front panel needs. The illustration above shows just a few of the almost endless variations possible from each master panel.

Unlimited Graphics Available

The flat, smooth, front panel surface permits unlimited choice of graphics. Functions may be grouped by color, with 480 colors available. Thirty choices of type style and size. And whatever visual symbols meet your specific needs.

THIS IS MONOPANEL:

- A complete touch switch sub-assembly, ready to mount.
- All switches and graphics on a .075″ thin panel.
- Flat, spill-proof surface wipes clean.
- Noiseless.
- 100% tested.
- Choice of terminations.
- Operating voltage: 50 V max.
- Operating current: 100 mA max.
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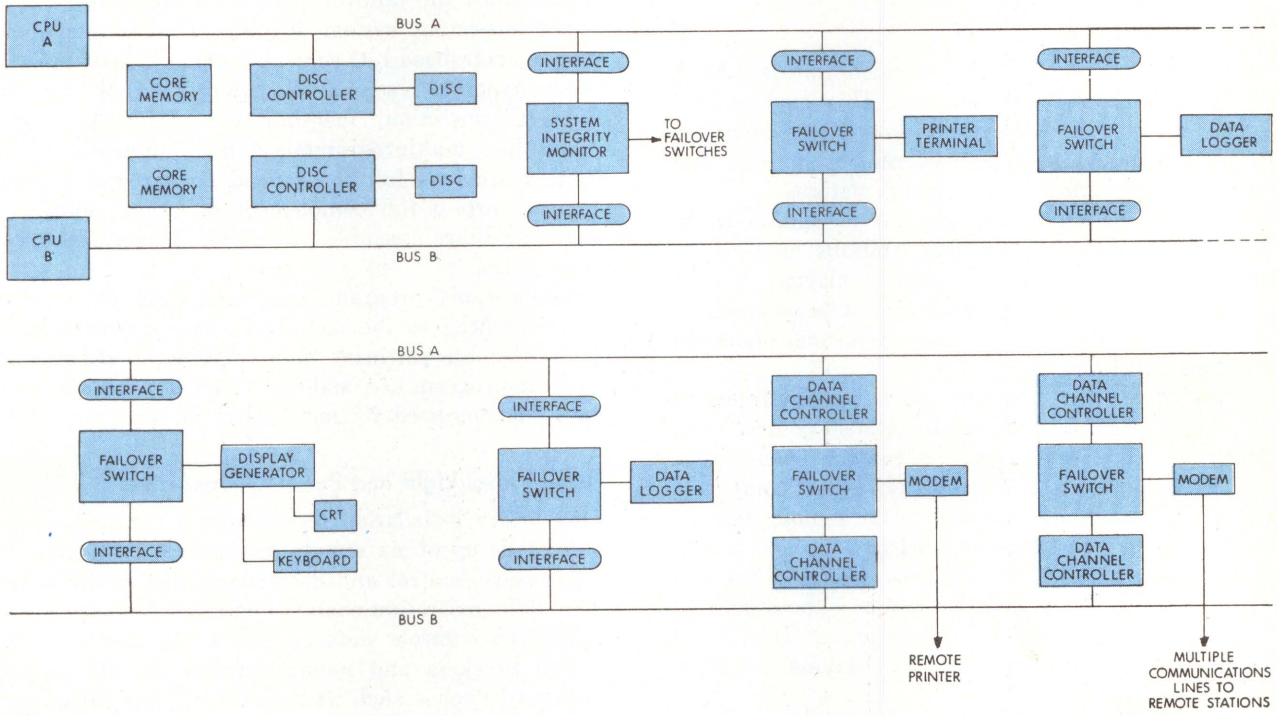


Fig 1 Functional diagram of typical SEMS master station. Fully redundant system includes two PDP-11 computers with core and bulk disc memories. System integrity monitor controls failover switches to shift control of dual-port peripherals to second computer if online CPU malfunctions. Manual switch (not shown) permits operator to assume full control if necessary

plus varied input/output (I/O) units as needed for the particular application. Expansion capability is provided by including a number of fully equipped and wired spare slots. These spares can be made operational by adding a plug-in card and I/O assembly—without internal wiring modifications.

Several remotes can be connected to the same communication line, generally determined by the existing line configuration and the response times required from the individual remotes. Communication lines are interfaced to the computer through a data channel controller (DCC) and a modem. The DCC is basically a serial-to-parallel/parallel-to-serial converter for receiving/transmitting. Each communication line (or groups of communication lines) is coupled to the buses via a peripheral interface controller and redundant DCCs.

Security of CPU-remote station communication is maintained through use of a modified Bose Chaudhuri (BH) cyclic check code which also affords efficiency in message transmission. Checking and generation of BCH code required in data exchanges is performed by a check code calculator (CCC) card interfaced to the CPU. The CCC performs the BCH calculations and can handle many DCCs.

Automatic Generation Control

Basic purpose of the automatic generation control (AGC) system is to assign automatically controlled generation such that a desired interchange schedule is maintained and the generation is done as economically as the interconnected system conditions permit. At frequent intervals SEMS scans the distribution system to determine actual tieline power flow, area frequency deviation, and output power of each generator.

Three software subsystems are included in AGC: load frequency control (LFC), interchange scheduling (IS), and economic dispatch (ED). Tieline power flows and frequency deviation are used by the LFC subsystem in the calculation of area control error (ACE), measured in units of power. ACE is the total error between the interchange being demanded and that being supplied.

Each area in an interconnected system is responsible for minimizing ACE at all times. When ACE is determined to be some value other than zero, the LFC subsystem distributes the error in power needed among the controllable generators. To alter the scheduled interchange power, the IS subsystem enters new scheduled interchange data, computes the net interchange power, and transmits schedule change data to the LFC subsys-

tem. Interactions among AGC operator, AGC subsystems, and the power system are shown in Fig 2.

Operating Functions

An interactive online editor is provided for data base, report, and log component changes. This enables user personnel to expand the system data base, including station and point address for new remote stations, and to expand point address for existing stations.

An inhibit function allows a point or station to be removed from scanning so that stations undergoing maintenance will not trigger persistent alarms. Also, a tagging function removes selected circuit breakers from system control without interference to normal operation of all other functions.

Training mode is a separate operating procedure. It allows an operator to be trained for system control without affecting actual remote station control. The console makes all responses as if the operator were completely online, but no commands are sent to the remote stations. Operators can be completely trained in a pseudo hands-on mode prior to full control of the system. They can thereby become familiar with the system without causing erroneous operations due to inexperience. This mode can be set up from one console while having the other consoles in full control.

System Software

Standard software operating system for SEMS operation is based on Digital Equipment Corp's RSX-11 which provides all services required for a real-time environment. These include scheduling, program status and communication, interrupt handling, mass storage control, real-time clock maintenance, and watchdog timer maintenance for failover peripheral switching.

The operating system furnishes quick interrupt response, centralized I/O control, automatic program scheduling, dynamic resource allocation, internal diagnostics for I/O operation, real-time debug facilities, system generation, multiprogramming, and automatic failover. It also provides full foreground/background capability and supports a full complement of system software including editor, assembler, compiler, loader, debug, and diagnostics.

Applications programs are modularly designed and are referenced to the data base. The system data base centralizes all pertinent data, making it readily available for program use, and eliminates duplication of common data accessed by more than one program.

Eastern Iowa Light and Power Cooperative

This SEMS installation monitors and controls a service area made up of six remote substations. It includes both supervisory control and data acquisition (SCADA) and automatic generation control (AGC).

SCADA controls status of 2-position devices such as circuit breakers and motor switches as well as multi-position switches such as transformer tap changers. An

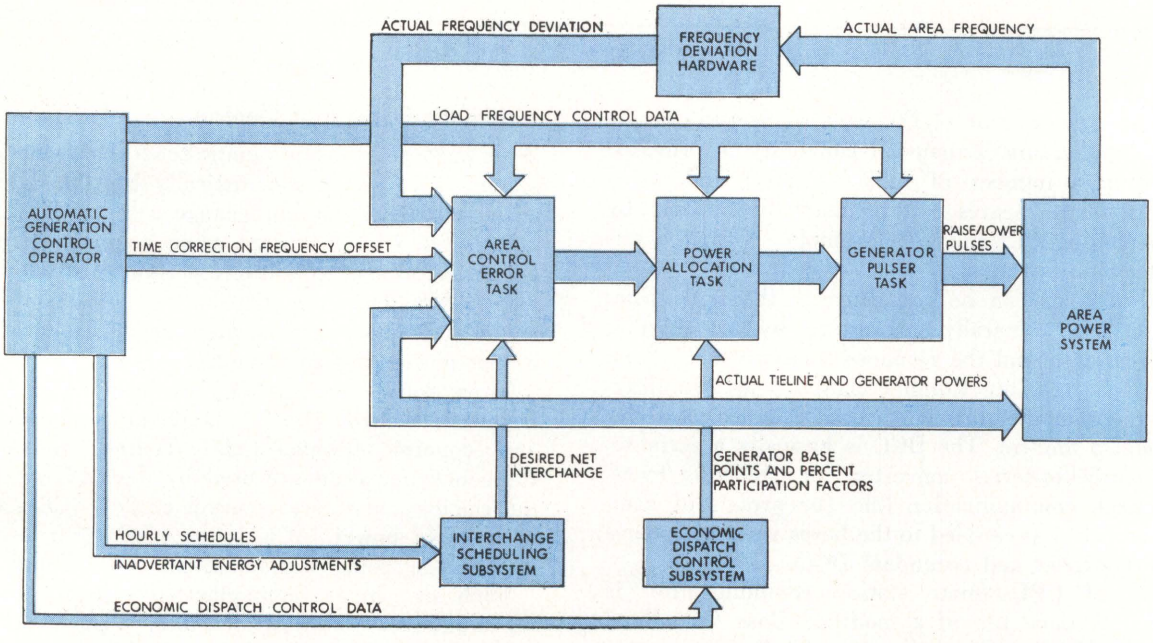


Fig 2 Automatic generation control (AGC) interactions among operator, subsystems, and power system. Broad arrows indicate flow of control information; medium width arrows show information flow from AGC operator; narrow arrows indicate secondary paths of information flow

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the most advanced new products from Intel's Intellec® Microcomputer Development System family, including the exciting new 888...

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The Intellec System 888 is the new development package which provides all the resources necessary to develop microcomputer system software in assembly language or in Intel's high level programming language, PL/M-80. Included in the system are the MDS-800 with 64k bytes of RAM and resident PL/M-80 high-level language compiler, the new MDS-DDS 1-million byte capacity Dual Drive Double Density Diskette Operating System, and the MDS-CRT. It's available now.

The Intellec MDS-800 supports the development and implementation of Intel 8080, 8085, 8748, 8048, 8035 and Series 3000 microcomputers. It includes an 8080A CPU, a universal bus with multiprocessor and DMA capability, an 8-level maskable priority interrupt structure, a real-time clock, 256-byte bootstrap loader, 2k bytes of ROM memory, 16k bytes of RAM, and interfaces for a teletypewriter, CRT, high-speed paper tape reader, high-speed tape punch, line printer and Universal PROM programmer. Standard software includes a ROM-resident system monitor, a RAM-resident 8080/8085 assembler and a text editor. It's available now.

The Intellec MDS-016 is a 16k RAM option, consisting of a model 2107 N-Channel dynamic RAM. It's available now.

The Intellec MDS-PTR is a High-Speed Paper Tape Reader peripheral, including a cable assembly and featuring a transfer rate of 200 cps. It's available now.

The Intellec MDS-PRN is a High-Speed Printer peripheral. The 5×7 matrix line buffered printer operates at a maximum of 165 cps. Line width is switch-selectable from 80 columns at 10 characters/inch to 132 columns at 16.5 characters/inch. The printer produces an original plus four copies and includes a tabletop cabinet, power supply, interface cable, operator lights, automatic on-off motor control and a 2-channel VFU control. It's available now.

The Intellec MDS-DDS is a Dual Drive Double Density Diskette Operating System for MDS-800 direct access bulk storage. It includes an intelligent controller and two Diskette Drive Units (each with 500,000 byte capacity), a cabinet, power supplies, cable assemblies and two ISIS-II system software Diskettes. ISIS-II includes a Relocating Macro-Assembler, Linker, Object Locator, Text Editor and Library Manager. The DDS is expandable to 2-million bytes. It's available now.

The Intellec MDS-CRT is a Keyboard Display Unit providing total user communication with all Intellec Diskette software and peripherals. The keyboard is detachable, and the RS232C-compatible CRT provides asynchronous data transfer rates of up to 9600 baud and features cursor positioning and cursor homing capability. It's available now.

The Intellec MDS-80-ICE is the famous In-Circuit Emulator which allows the design, development and debugging of a product in its own real-time operating environment. The ICE module consists of an 8080 CPU In-Circuit Emulator and includes a cable assembly and interactive software. It's available now.

The Intellec UPP-101 is a Universal PROM Programmer, including a cabinet, software, power supplies, cable and one 16/24-pin zero insertion force PROM programming socket pair. At least one "personality card" is required. It's available now.

The Intellec UPP-816 is a Personality Card for the 2716 2k × 8 EPROM, which features a 450 nanosecond access. It's available now.

The Intellec UPP-848 is a Personality Card for the new 8748 single-chip LSI microcomputer. The card includes an adaptor socket. It's available now.

The Intellec UPP-855 is a Personality Card for the new 8755 PROM (a pin-for-pin equivalent of the 8355 ROM) which contains 2k bytes of program memory, an address latch and two 8-bit general purpose I/O ports (one of which may be used to address external memory). It's available now.

The Intellec MDS-PLM is a Resident Compiler for Intel's High Level Programming Language, PL/M. It translates a source program written in PL/M into machine code for the 8080A and 8085 microcomputers. An MDS-DDS and 64k bytes of RAM are required. It's available now.

The Intellec MDS-D48 is a Support Package for assembling 8748, 8048 and 8035 single chip microcomputer programs on the MDS-800. It's available now.

The Intellec PROMPT-48™ is a Personal Programming Tool for the 8748 and 8048. It runs programs in real-time, with multiple breakpoints, or with single-stepping. PROMPT-48 includes both 8748 and 8035 CPUs, an EPROM Programmer, an integral keyboard, displays and system monitor in ROM. The system provides 64 bytes of RAM register memory, 1k bytes of EPROM program memory, 256 bytes of RAM data memory and 1k bytes of RAM program memory. System I/O, bus and memory can be expanded or directly interfaced to a user prototype. It can be used as a stand-alone system, or it can work with any terminal. It may be connected to the MDS-800 for direct program downloading and includes I/O ports, a bus cable and comprehensive documentation. It's available now.

The Intellec PROMPT-SER is a serial cable for connecting PROMPT-48 to a TTY or CRT. It's available now.

The Intellec PROMPT-SPP is a Specialized EPROM Programmer Kit which allows PROMPT-48 to be connected to the MDS-800 as a specialized EPROM programmer peripheral or debugging station. It's available now.

You can rent any of these products—from stock, immediately—by contacting

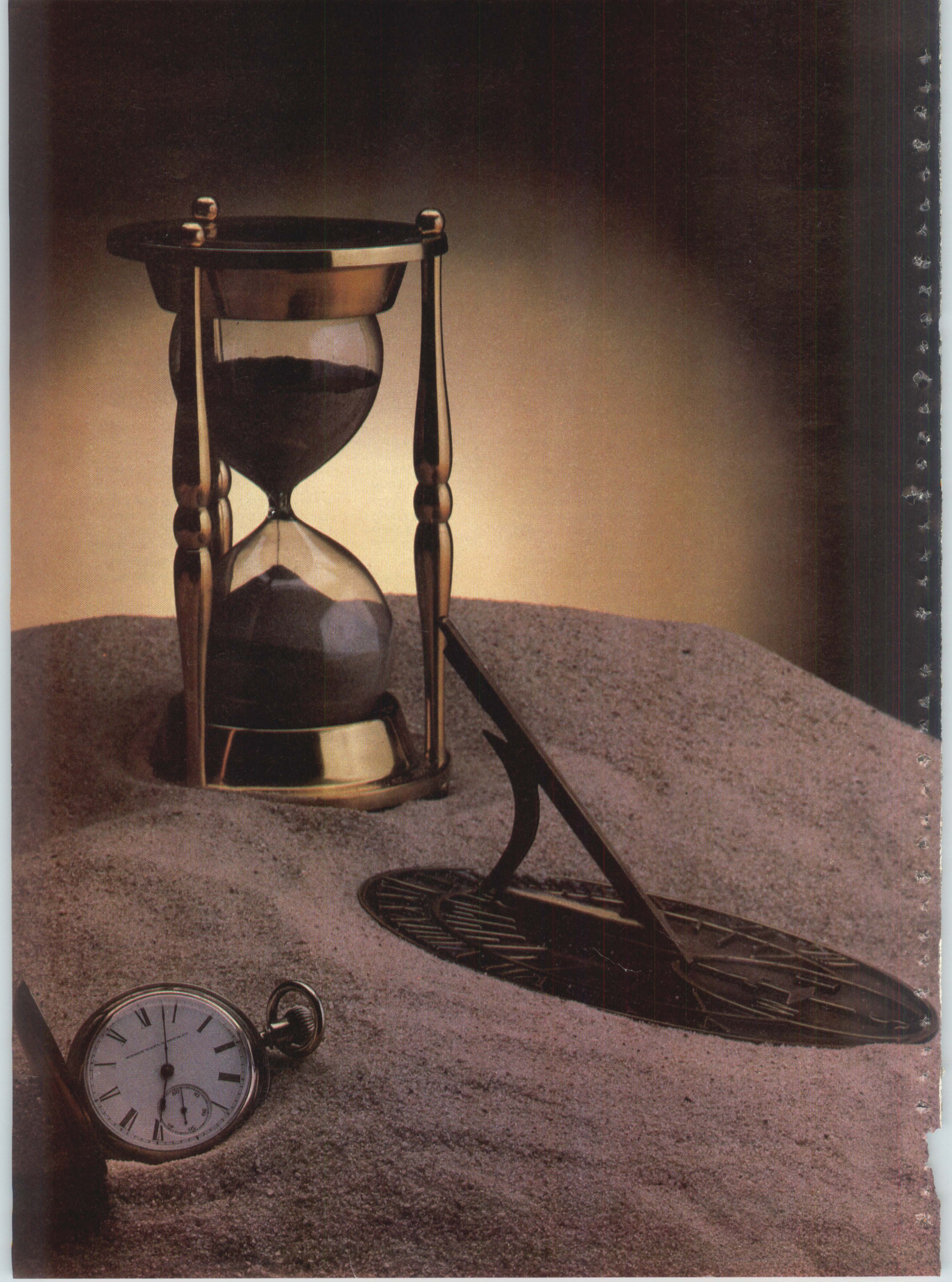
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Systems computers fit the term "minicomputer" in price alone. If your application is performance-sensitive, we'll save you money. If you're budget-sensitive, we'll give you more performance for your dollar.

The SEL 32/35 can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including control processor with floating-point arithmetic, memory, chassis, power supplies and cabinet.

The SEL 32/55 is offered in a variety of both single and multiple CPU configurations, with from 32K bytes to 1 million bytes of 600 nsec memory.

The SEL 32/75, with up to 16 million bytes of main memory, has a concept so new, we had to coin a special term to describe one of its main features: Regional Processing Units. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating- Point Hardware and Writeable Control Storage.

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alarm sounds if a device does not respond within a set period of time after a command is issued. SCADA also monitors and reports on equipment status and provides digital telemetering of analog measurements. AGC controls the output of two power generators as well as power flow from and to four utility interconnections.

Master station hardware at this facility consists of two PDP-11/40 computers, three disc memory units of 1.2M words each, programmer console, three CRT/keyboard operator consoles, remote station communication channels, alarm and events logger, data logger, mapboard interface, recorder interface, high speed reader/punch, frequency deviation transducer, and two teleprinters. Data base size limitations to include more substations are expandable by addition of core and/or disc memory units.

Oklahoma Gas & Electric Co

A 75-mi^2 area involving 100 generation, transmission, and distribution substations will be supervised and controlled by this SEMS facility. Initially, 14 remote terminal units were installed but the system is being expanded at a rate of 10 units a year until it reaches a total of 100.

Two PDP-11/35 computers serve as CPUs. The master station contains four consoles. Three, for use by two operators and the dispatcher, are identical; each includes 7-color CRT display, alphanumeric control keyboard, and light pen. However, controls on the dispatcher's console will normally be inhibited. Three General Electric Terminet 1200s are used for periodic and alarm logging.

The programmer's console contains 7-color CRT, keyboard, light pen, teletypewriter, card reader/punch, and line printer. It provides access to the offline computer for program update, engineering study, training, or maintenance.

Each CPU has access to 64k words of 16-bit core memory and a 1.2M-word disc memory. An "alternating



device" feature allows operators to assign multiple tasks to a single peripheral. This enables one peripheral to assume the functions of another peripheral that becomes disabled. This shift in responsibility occurs without disruption of logging functions.

Corpus Christi Central Power and Light Co

This Texas utility went online in late 1976. It supervises and controls power transmission and distribution to approximately 370,000 residential, commercial, and industrial customers. Facilities include master control center, remote dispatching station, and 16 substations.

The control center in Corpus Christi (Fig 3) contains dual PDP-11/35 computers, two operator consoles with CRT displays and keyboards, two teleprinters, paper tape reader/punch, and logger. Consoles and logger are 10 miles apart.

Operators control circuit breakers, transformers, and motor-operated switches from the consoles using a 3-step select-before-operate process. However, service per-

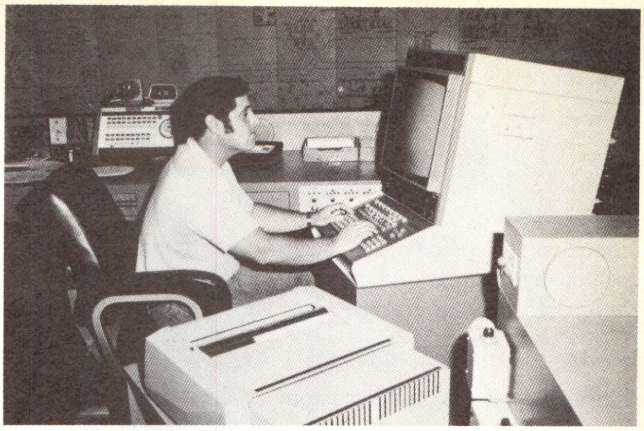
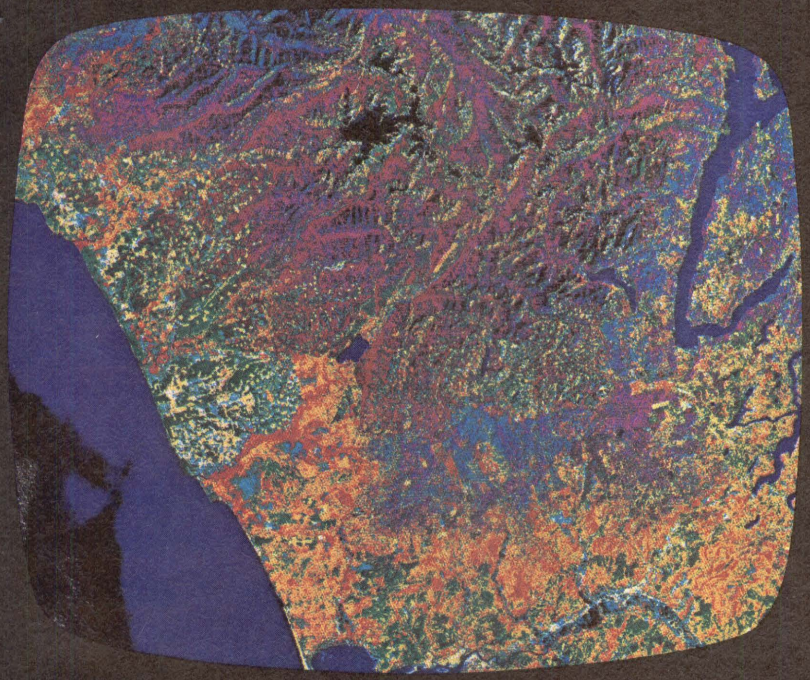


Fig 3 Master control center of Central Power and Light Co SEMS installation in Corpus Christi, Texas. Status of transmission and distribution functions is displayed on CRT in 7-color display, in either tabular or schematic format. Command to alter status of any control point is entered through keyboard



This display shows the Quinault Indian Reservation in Washington state. 16 separate colors have been assigned for such categories as Burn Areas, Forest, Brush and Bare Land.

Bendix Aerospace Systems Division uses a Ramtek display generator to really show its colors. The Bendix Multispectral Data Analysis System (M-DAS) provides a clear, color-coded display for analysis of data from NASA's LANDSAT. And by using Ramtek's moving window display—or scroll—they're able to look at more data at one time than can be displayed on the still screen. Images of the same areas may also be correlated so that changes between past and present can be referenced.

Bendix is but one of a growing number of customers who are finding that Ramtek's modular graphics and imagery systems are giving them the expandability, flexibility and increased productivity they need. Besides the basic alphanumeric and imaging capability, Ramtek offers a wide variety of other functions including graphics — vectors, conics, plots, bar charts — pseudo color and grey scale translation.

Because the Ramtek RM 9000 family is totally controlled by a standard 8080 microprocessor, it is easy to develop and download your own control software.

To find out more about how Ramtek can show off for you, call or write: Ramtek Corporation, 585 North Mary Avenue, Sunnyvale, California 94086; (408) 735-8400.

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sonnel are protected when performing remote site maintenance by a "tagging" feature which prevents the operators from closing any device at that site.

Jacksonville Electric Authority

Approximately 200,000 customers in the Jacksonville area of Florida are currently served by a SEMS electrical transmission and distribution facility (Fig 4). Operators can monitor power network data transmitted to the master station from 45 substations and three tielines with Florida Power & Light. Future plans include automatic control of electrical loading of 11 fossil fuel steam turbine generators and 14 gas turbine peaking units. Computers in this system are PDP-11/40s. Orders to system control points are initiated via light pens. An operator touches a light pen to a display of the control point on the CRT screen, presses an operate button, and the order is relayed to the control point.

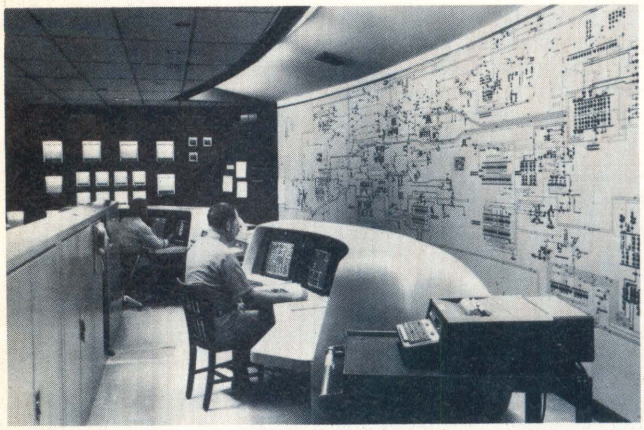


Fig 4 Jacksonville, Florida SEMS facility. Elliptically-shaped operator consoles contain CRTs and keyboards. Light pens are used in this SEMS installation to pinpoint control point on CRT. Button on keyboard is then pressed to initiate command to that control point

Metropolitan Water District of Southern California

A much different application of SEMS techniques will be installed in southern California to monitor and control three water processing plants and a water distribution network. Three computer systems will provide central control capability at the Riverside and R. A. Skinner Water Filtration Plants in Riverside County and the F. E. Weymouth Softening and Filtration Plant in Los Angeles County.

Part of the overall plan includes a pilot project to completely automate the Riverside plant so that it can be remotely controlled from the R. A. Skinner plant. Computer software will manage the filter backwash operation, reclamation water processing, service water supply, processed water reservoir level control, and plant power consumption entirely without the intervention of human operators.

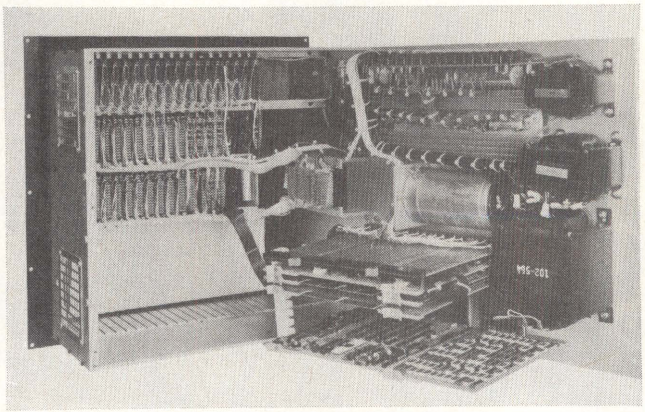
Remote sensing devices will provide data to enable supervision and control of gates and valves throughout the plants and the distribution networks. Status information transmitted from the sensors will be processed by the computers and displayed on color video screens in the master control centers. Operators will be able to exercise remote control from associated keyboards.

Each of the three master stations will include dual PDP-11/34 computers and associated core memory, four disc drives with 4M words of bulk memory (combined moving and fixed head devices), two operator consoles with CRT displays and keyboards, two trending units, two video copy units, two magnetic tape drives, and two line printers.

Circle 160 on Inquiry Card

DC&AS BRIEF

DNC Unit Offers Multi-Axis Control



Direct numerical control for up to eight parameters is reportedly attainable with the System IV DNC unit manufactured by Unico, Inc, 3725 Nicholson Rd, Franksville, WI 53126. Both the CPU, a general-purpose minicomputer, and associated I/O options are mounted in a single enclosure.

When combined with the company's real-time system—RTS-II—for multilevel application programs, the unit recognizes instructions of the DEC PDP-8 computer. For normal operation, the unit is in run mode; a load mode is used to enter diagnostic and application programs and system data. Diagnosis of hardware and software problems is accomplished in test mode.

Basic memory is 8k words; three 8k RAM expansion boards are available to provide a total of 32k words. Other major components include data input keyboard, a 16-pushbutton panel for manual data entry; 18-readout data output display for presenting data from the processor or memory; 10-module data input station for converting external inputs and transferring data to the processor or memory; 10-module data output station for transferring data to external devices; and 150-char/s paper tape reader for loading operating programs, system variables, and diagnostic procedures into the memory. A parallel computer data bus enables easy system expansion. □

Multi-User/Multi-Task DOS

COMMAND PERFORMANCE



muPro-80D Multi-User, Multi-Task Disk System

Software

- Concurrent Multiple Terminal Operation
- Multiple Task Real-Time Operating System
  - Supports up to 256 concurrent tasks
  - Provides 64 priority levels
- Program Overlay Capability
- Comprehensive File Management
  - List File Directory
  - Add, Delete, Rename, Append File
  - Run-Time file definition
- File Utilities: Copy File
  - Copy and Compress Disk
  - Format Disk
- I/O Device Characteristics transparent to user
- Concurrent Interrupt-Driven I/O
- Calendar Maintenance - Date, Time
- Supports BSAL-80, Linking loader and Text Editor
- Operating System Requires 16K Bytes

Hardware

- Dual Diskette Drive - 512K Bytes
- Soft Sectored - IBM 3740 compatible
- High Speed Seek - 76 track seek in 100mSec.
- Single Card Controller installs directly into muPro-80 chassis
- Double-Sided Recording - Optional
- Controller accomodates up to two dual drives (four diskettes), or four single drives
- Real Time Clock
- Write Protect
- Manual or Processor controlled diskette eject
- Data transfer via DMA
- Small Size - 4.6"H x 10.0"W x 21"D including power supply. 32 lbs.

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Mostek takes you forward to a new era in low power systems.



Introducing the Edge-Activated™ Series.

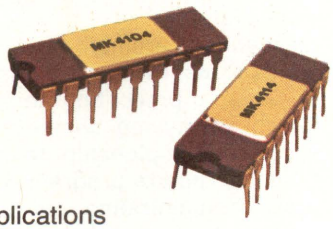
Higher density, lower power and simplified system design. That's the idea behind Mostek's Edge-Activated Series. The series includes a complete family of high-density static RAMs and ROMs, with a wide selection of organizations. All devices are implemented with the same edge-activated circuit design concept which allows you to design a +5V only system without compromising speed or power. It's the best of both worlds.

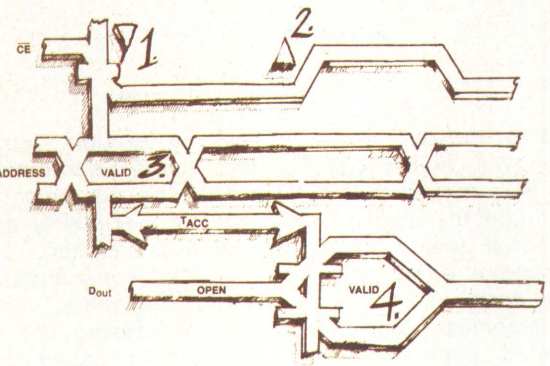
Proven design techniques for maximum performance.

Mostek's approach integrates a static MOS storage cell with dynamic MOS periphery so that the full advantages of the technology can be realized. Now your applications can be implemented with a minimum number of devices. Also, edge-activated devices operate at faster speeds than traditional static circuits but with much lower power dissipation.

Other system benefits include . . .

- totally static operation—no refresh required
- single +5V power supply—±10% tolerance
- on-chip address latches
- active and standby power—lowest in the industry
- reduced V_{CC} for battery back-up applications
- direct TTL compatibility and common I/O operation



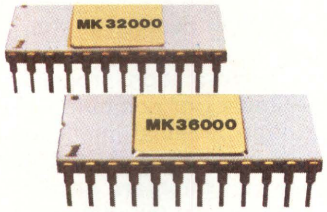


A simple high to low transistion at the Chip Enable input (1) activates the entire family of memory devices. Returning the CE input to a high level (2) achieves a 75% reduction in device operating power for an automatic standby power mode. Address information is strobed and latched (3) into a set of on-chip registers, thereby eliminating "set up" time requirements and minimizing "hold" time. While data is valid (4) you have full control of the Data Output.

Let's put a dollar value on lower power.

One common timing signal, provided in almost every memory application, activates the entire family of devices. However, if the clock signal must be provided externally, the system benefits of lower power far outweigh design complexity. An example is a 16K × 9-bit storage matrix. Designed with edge-activated MK 4104's, this system would dissipate less than 1 watt in the memory array, while the same system with static-interface RAMs would dissipate approximately 18 watts. Since typical power sub-system designs cost from $1.00 to $1.50 per watt, both design and cooling costs are reduced significantly.

Data Sheets, Application Notes, price and delivery are available from Mostek field sales representatives.



The Edge-Activated™ Series

	Access Time (max)	Active Power (max)	Standby Power	Industry Standard Pin Configuration
MK4104 (4K×1 RAM)	200 ns	120 mW	30 mW	18 pin
MK4114 (1K×4 RAM)	200 ns	120 mW	30 mW	18 pin
MK32000 (4K×8 ROM)	300 ns	200 mW	25 mW	24 pin
MK36000 (8K×8 ROM)	300 ns	200 mW	25 mW	24 pin

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IFIP Congress 77



Toronto, Canada
August 8-12

The 7th IFIP Congress 77 is based on the theme of "The Maturing Profession—Perspectives and Prospects," gathering professionals in the computer industry to discuss, analyze, and evaluate the state of computer sciences on an international level. Concerned with the indepth coverage of computer systems technology, automated information systems, and social issues of computer applications, the technical program features invited speakers, contributed papers, and panels/minisymposia, placing particular emphasis on the practical aspects of the field. Program Committee Chairman is Prof Wlad M. Turski of Poland; Chairman of the Organizing Committee is James H. Finch of Canada.

Sponsored by the International Federation for Information Processing, the Congress features topics covering diverse branches of information processing: an assessment of the future impact of computer-aided design; the status of research in artificial intelligence; and the problems of information processing and management, as well as the changes which are necessary based upon an overview of theoretical foundations and education. Issues of data base organization will be debated, in addition to the areas of applications in science and engineering, computer software, networks, and recent developments in hardware, with particular emphasis on such subjects as fault tolerance, large capacity memories, and microprocessors. Excerpts of the technical program, which consists of six parallel sessions, were outlined in last month's issue of *Computer Design*. A full Conference at a Glance, together with a guide indicating where to eat, what to see, and what to do while in Toronto, is contained in this issue for the reader's convenience.

Exhibits

To complement the technical program, a 4-day exhibition is scheduled on Monday from 11 am to 6 pm, and Tuesday through Thursday from 9 am to 6 pm, to be held at the Sheraton Centre. On exhibit will be data processing equipment and systems, major computer services, peripheral equipment, and material directly related to handling, storage, and care of data serving industrial, commercial, and professional fields of the world. Engineers, designers, financial management, data processing users, and other visitors will view firsthand the latest developments and trends in peripherals and data entry systems, plus a comprehensive range of design applications, software, and services.

Registration and Activities

Registration fee is $145 which includes materials, a copy of the proceedings to be distributed at the Congress, and admission to the technical sessions and exhibition. Registration will take place at the Royal York Hotel.

Opening ceremonies will be held Monday morning with Dr Josef Kates, Chairman of the Science Council of Canada, presenting an address. Also scheduled are 12 chess playing computer programs entered in the second championship tournament of the world. The Science Theatre program will present movies and video tapes concentrating on specific areas denoting the current state of information processing.

Social highlights of the week include a Welcoming Reception on Sunday evening and a Wine and Cheese Social on Monday evening. Optional plans offer choices of a picnic or a harbor cruise and dance on Tuesday and Wednesday evenings. Thursday evening's activities will begin with a reception, followed by a banquet, entertainment, and dancing.

Further information on the IFIP Congress 77 may be obtained from the U.S. Committee for IFIP Congress 77, Bowery Savings Bank, 110 E 42nd St, New York, NY 10017.

Now Norden gives DIGITAL's PDP-11/34 even more military muscle with CACHE memory.



CACHE memory increases PDP-11/34M throughput up to 100%.

On full ATR versions of the military PDP-11/34M minicomputer, a 1K CACHE memory enhancement is now available as a plug-in, double card module. Completely transparent to programmers, it sharply increases price/performance, boosting throughput up to 100%. Shipments start in the fourth quarter of 1977.

PDP-11/34M uses exactly the same software as commercial PDP-11/34.

First in a new family of militarized computers, the PDP-11/34M combines Norden's experience in military electronics with DIGITAL architecture and DIGITAL software.

The result is the PDP-11/34M, a fully militarized mini-computer designed and tested to meet all mil specs—airborne (MIL-E-5400), shipboard (MIL-E-16400) and land (MIL-E-4158). It's available in half or full ATR chassis and with a wide range of militarized peripherals.

This new system uses the identical software as the commercial PDP-11/34—same applications software, same support software, same operational software. You save time and money on development, training and operations. You start with a time tested software system as well as a proven hardware system.

First shipments go out in July 1977.

For more information, call or write Director of Marketing, Computer Products Center, Norden Division, United Technologies Corporation, Norwalk, CT 06856. Telephone (800) 243-5840 toll-free, or call (203) 838-4471.

PDP-11 data processing with Norden military muscle.

NORDEN

Division of
UNITED TECHNOLOGIES.

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Where To Eat

The restaurants listed below are located in the Midtown-Downtown areas. Many other fine restaurants can be found outside of these areas. *Computer Design* is publishing this list as a guide and quick reference, with no intention of recommending any restaurant as to economy or quality of food.

BARBERIAN'S STEAK HOUSE, 7 Elm. Downtown. Steaks and seafood served in warm, early Canadian environment. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5 pm-1 am, Mon-Sat; 5 pm-midnight, Sun. (597-0335)

BARDI'S, 56 York. Downtown. Shish kebob, Steak Tartare, lobster tails, and prawns highlight menu. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5:30-11:30 pm, Mon-Sat. (366-9211)

CAFE MADRID, 42 Hayden. Midtown. Quiet, elegant Castilian restaurant offers Spanish cooking such as Polla Costa Brava and Paella Valenciana. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5:30-11 pm, Mon-Thurs; to 1 am, Fri and Sat. Closed Sun. (922-3151)

CAPTAIN JOHN'S, One Queen's Quay W (Foot of Yonge). Downtown. Seafood au Whiskey, curried shrimp entice patrons aboard city's only floating restaurant. Steak for landlubbers. Cheese and grapes are on the house. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5:30-10:30 pm, Mon-Thurs; to 1 am, Fri and Sat; noon-10 pm, Sun. (363-6062)

CASA BALDO, 15 St Andrews at Spadina. Downtown. Spanish oasis in the heart of Kensington Market. Menu includes gazpacho, seafood in casserole, stuffed veal, and paella. Lunch, 11:45 am-2:15 pm, Tues-Fri; Dinner, 5:30-10:30 pm, Tues-Fri; to 11 pm, Sat; 5-10 pm, Sun. Closed Mon. (362-7535)

CHATEAU D'ORSI, 712 Bay. Downtown. Specialties from the south of France include Beef Bourguignon, Dover Sole, and rabbit. Lunch, 11:45 am-2:15 pm, Mon-Fri; Dinner, 5:30-10:15 pm, Mon-Thurs; to midnight, Fri and Sat. (595-1785)

CICCONE'S, 601 King W. Downtown. Italian cuisine with continental atmosphere. Lunch, 11:30 am-2:30 pm, Mon-Fri; Dinner, to 1 am, Mon-Sat. (368-5037)

COPENHAGEN ROOM, 101 Bloor W. Midtown. Lunchtime offers profusion of open face sandwiches, and dinner centers on genuine French and Danish dishes. Open 11:30 am-11:30 pm, Mon-Sat. (920-3287)

CORNUCOPIA, 101 Richmond W. Downtown. Greenhouse setting provides pleasant atmosphere in which to enjoy varied menu. Open 8 am-midnight, Mon-Sat. Dinner served 5:30-midnight. (360-1954)

CSARDA, 720 Bay. Downtown. Serenades of gypsy violins and flaming platters of Transylvanian treats such as goulash, chicken paprika, and apple strudel contribute to the warm atmosphere. Lunch, noon-2:30 pm, Mon-Sat; Dinner, to midnight, Mon-Sat; 5-10 pm, Sun. (597-0801)

DOOLEY'S, 23 Bloor E. Midtown. Try Mrs Murphy's clam chowder, Irish stew with dumplings, or corned beef and cabbage, along with imported spirits. Open for lunch, dinner, and late night snacks. (922-2626)

DR ZHIVAGO'S, 345 Bloor E at Sherbourne. Midtown. Authentic Russian cuisine which includes chicken Tabaka, Shashlik, Beef Stroganoff, Blini with Red Caviar, and Sturgeon à la Petersburg. Lunch, noon-3 pm, Mon-Sat; Dinner, 5 pm-1 am, Mon-Sat; to 10 pm on Sun. Reservations required Thurs-Sat. (961-5511)

ED'S WAREHOUSE RESTAURANT, 270 King St W. Great atmosphere. Roast beef specialties. (363-4211)

EL TORO, 39 Colborne. Downtown. Spanish-style steakhouse with an abundance of appetizers and hot cheese garlic bread. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5 pm-1 am. (368-2418)

FISHERMAN'S WHARF, 145 Adelaide W. Downtown. Cruise ship setting is fitting backdrop for tidal wave menu which boasts of 60 items. Lunch, noon-3 pm, Mon-Fri; Dinner, 5 pm-1 am. (364-1344)

GASTHAUS SCHRADER, 120 Church. Downtown. Teutonic fare and German beer in country inn environment. Lunch, noon-2 pm, Mon-Fri; Dinner, 5-10 pm, Mon-Sat. (364-0706)

HUNGARIAN HUT, 127 Yonge. Downtown. Gaily decorated room is setting for cabbage rolls, wiener schnitzel, and other Hungarian specialties. Live entertainment provides romantic dinner music. Open 11:30 am-11 pm, Mon-Sat; to 10 pm on Sun. (864-9275)

HUNGARIAN VILLAGE, 990 Bay. Midtown. Famous Hungarian hospitality awaits you, complete with gypsy violinist. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5 pm-midnight, Mon-Thurs; to 1 am, Fri and Sat; to 10 pm on Sun. (922-5401)

IMPERIO, 349 College. Downtown. Portuguese restaurant located in Kensington Market area serving native dishes. Lunch, noon-3 pm; Dinner, 6-11:30 pm, Mon-Sat; noon-10 pm, Sun. (922-0954)

JAVA, 14 Richmond E. Downtown. Indonesian restaurant specializing in rijstaffel, or rice table. Open noon-11 pm, Mon-Fri; 5 pm-midnight, Sat; 5-10 pm, Sun. (364-7666)

LA MAMOUNIA, 1280 Bay. Midtown. A true taste of Morocco. Couscous and mechoui are prepared from generations-old recipes. Open noon-1 am, Mon-Sat; 5-10 pm, Sun. (961-0601)

LA SCALA, 1121 Bay. Midtown. Italian cuisine with fresh pastries and rum cakes rounding out menu. Lunch, Tues-Fri; Dinner, from 5 pm, Tues-Sat. (925-1216)

LICHEE GARDEN, Upstairs, 118 Elizabeth. Downtown. Traditional Cantonese cuisine. Open 11 am-1 am, Mon-Thurs; to 3 am, Fri and Sat; to midnight, Sun. (364-3481)

MERMAID SEAFOOD HOUSE, 724 Bay. Downtown. One of Toronto's first seafood houses with a menu prepared by experts. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5:30-10 pm, Mon-Thurs; to midnight, Fri and Sat. (597-0077)

MICHI, 459 Church. Downtown. Practice with chopsticks on Japanese tempura or sukiyaki. Forks available if needed. Lunch, Mon-Fri; Dinner, from 5 pm daily. (924-1303)

MR I'S, 65 Queen W. Downtown. Downstairs delicatessen-restaurant is a food lover's delight, specializing in Jewish style food. Open 8 am-7 pm, Mon-Sat. (361-1209)

MOORINGS, 404 Yonge. Downtown. Toronto's first seafood house menu includes scampi, lobster, frogs legs, Arctic Char, and bouillabaise. Open noon-midnight, Mon-Sat. (597-0737)

NAGS HEAD I & II. True English pub atmosphere and cuisine complete with draught beer, roast beef sandwiches, steak and kidney pies, and fish and chips. Live entertainment. 7 King W. Open 8 am, Mon-Sat; noon, Sun. (366-1194). 74 York St. Open noon-1 am, Mon-Sat. (368-6874)

NANKING TAVERN, 75 Elizabeth. Downtown. Wide variety of exotic Chinese dishes. Open 11:30 am-1 am, Mon-Thurs; to 2 am, Fri and Sat; 4-11 pm, Sun. (363-4907)

NIKKO SUKIYAKI, 460 Dundas W. Downtown. Kimono-clad Japanese waitresses prepare sukiyaki, shrimp tempura, and beef teriyaki. Open daily from 4:30 pm. (366-2164)

OLD ANGELO'S, 45 Elm. Downtown. With specialties such as Scallopine Marsala, Veal Parmigiana, and Lasagne Verde. Open noon-1 am, Mon-Sat. (597-0155)

OLD SPAGHETTI FACTORY, The Esplanade behind O'Keefe Ctr. Downtown. A lavish and looney environment for spaghetti lovers. Open noon-midnight, Mon-Thurs; to 1 am, Fri and Sat; to 10 pm, Sun. (864-9761)

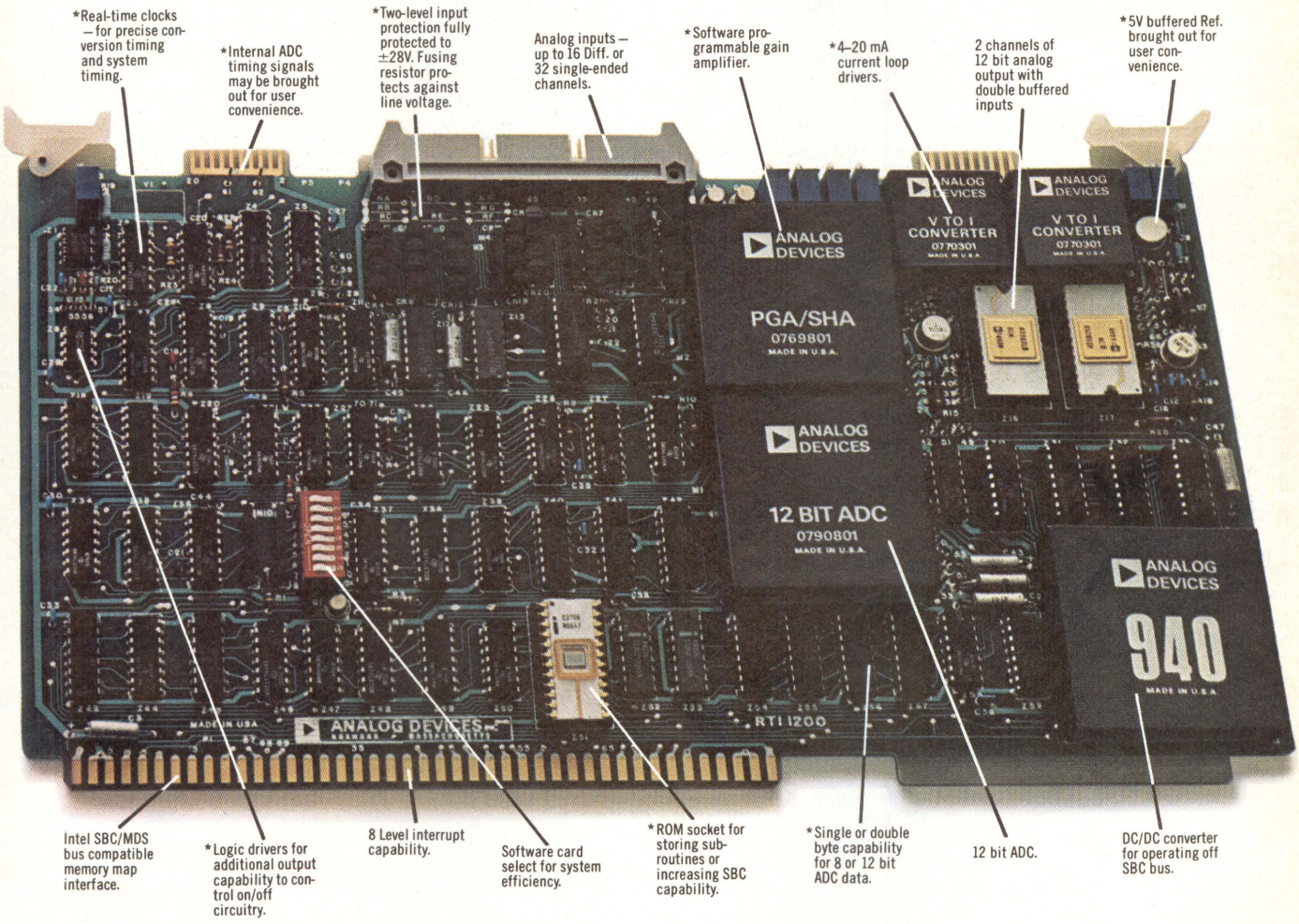
PEPPERMILL, 50 Cumberland. Midtown. Handsome dining room with comfortable English tavern chairs, mellow barn siding, and a menu with lots of latitude. Open, 11:30 am-1 am, Mon-Sat. (925-6277)

QUO VADIS, 375 Church. Downtown. Award-winning restaurant with grand style serves specialties of Dover sole with crabmeat, chicken Valdostana, Scaloppina Forestiere. Lunch, noon-2:30 pm, Mon-Fri; Dinner, 5-11:30 pm, Mon-Fri; to 1 am, Sat. (863-9900)

(*Continued on p 68*)

Important news for Intel SBC 80 users:

The RTI-1200 solves your real-time analog I/O subsystem problems.



Now Intel SBC 80 users have the most complete, most versatile and easiest-to-use input card for the acquisition and control of analog signals.

What you don't see here are all the other significant RTI-1200 features that enhance its maximum convenience and versatility. One of the most impressive is our User's Guide. It doesn't just tell you how to hook up jumpers. It does tell you how to write programs that optimize throughput rates, how to use the 8080's instruction set to take advantage of the RTI-1200's capabilities and a whole lot more.

If you're looking for the solution to your analog I/O interface problems, the Analog Devices' RTI-1200 is it. Single prices range from $629 to $979 depending on options (quantity discounts are available). The Analog Devices' RTI-1200, the first in a family of analog subsystems from the market leaders in analog products for signal conditioning, converting and control.

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SHOPSY'S, 295 Spadina. Downtown. Corned beef, pastrami, Matsoh-ball soup, and kishke highlight menu. Open 10:30 am-8 pm, Mon-Thurs, Sat, and Sun; to 3 pm, Fri. (366-5401)

SILVER RAIL, 225 Yonge. Downtown. Attentive waiters serve beef stroganoff and roast beef while you dine among Victorian heirlooms. Open noon-1 am, Mon-Sat. (368-8697)

TERRACE, 146 Yorkville (York Sq). Midtown. Extravagant selection of 52 crepes, clubhouse sandwiches, and after-theatre fondues. Open 8:30 am-1 am, daily. (920-5115)

TOM JONES STEAKHOUSE, 17 Leader Ln. Downtown. Classic steakhouse fare plus extensive wine list. Lunch, 11:30 am-2:30 pm, Mon-Sat; Dinner, 5 pm-1:30 am, Mon-Sat. (366-6583)

TOP OF TORONTO, CN Tower, 301 Front W. Downtown. Revolving restaurant atop CN Tower lets you see the world as you dine. Lunch, noon-2:30 pm, Mon-Sat; to 4 pm, Sun; Dinner, Mon-Sat, first sitting, 6 pm; second sitting, 9 pm; Sun, first sitting, 5 pm; second sitting, 8 pm. (362-5411)

WINSTON'S, 104 Adelaide W. Downtown. Dine in elegance where service is a time-honored tradition. Try the clear turtle soup or sherry Theodore with your entree of filet mignon, or duckling with black cherries and brandy. Lunch, noon-3 pm, Mon-Fri; Dinner, 6-11 pm, Mon-Sat. (363-1627)

Where to Relax

Toronto is filled with thousands of places to go and things to see. In addition to the tours planned by IFIP, *Computer Design* has compiled an abbreviated list which can be used as a guide. For complete information, especially regarding art, theatre, and music events, consult the daily newspaper.

TOURS

IFIP has planned several local tours, each of which departs from the Castle Harbour and Royal York Hotels. They are escorted and commentaries are provided on the majority of tours. Check IFIP handbook for specific details, especially departure times.

TOUR A—CITY OF TORONTO—Tour takes in the city's churches, City Hall, Ontario Parliament Buildings at Queen's Park, and the University of Toronto, as well as venturing into the beautiful residential area of Forest Hill. Casa Loma, the castle on the hill, High Park with superb gardens and horticultural displays, and Kensington Market are highlights. A brief stop is made at China Court. Length: 3½ hrs. Days: Mon, afternoon; Tues & Wed, morning and afternoon; and Thurs, afternoon. Cost/person $7.

TOUR B—McMICHAEL GALLERY—McMichael Gallery is actually in the town of Kleinburg, even though the tour commences with highlights of Toronto. The Gallery consists of 30 rooms constructed of fieldstone and timbers, situated in 600 acres of parkland, and is filled with precious art. Lunch is provided nearby at The Doctor's House and Livery. Length: 6 hrs. Days: 9:30 am, Tues, Wed, and Thurs. Cost/person $15.

TOUR C—NIAGARA FALLS—Travelling out of Toronto to Hamilton and St Catherines, and then heading south to the Welland Canal, tour covers intricate lock system, and time is spent at Niagara Falls where lunch will be served. The return journey goes through Niagara-on-the-Lake's orchards and vineyards. Length: 7 hrs. Days: 9 am, Tues, Wed, and Fri. Cost/person $16.50.

TOUR D—BLACK CREEK PIONEER VILLAGE—Just north of the city, one can experience living as it existed 150 years ago. Museum and exhibits plus villagers performing work they would have done a century ago. Lunch is served in the Old Mill Restaurant located in the Humber Valley. Length: 6 hrs. Days: 9 am, Tues, Wed, and Thurs. Cost/person $16.50.

TOUR E—SHERWAY GARDENS SHOPPING—Brief tour of city terminates at Sherway Gardens Shopping Centre, one of Toronto's newest indoor malls containing approx 195 stores and numerous gardens. Length: 5½ hrs. Days: 9 am & 10 am, Tues, Wed, and Thurs. Cost/person $4.50.

TOUR F—HAMILTON, NIAGARA-ON-THE-LAKE, AND NIAGARA FALLS—The Royal Botanical Gardens cover nearly 2000 acres and feature 25 miles of nature trails. Leisure time can be spent exploring Niagara-on-the-Lake. Dinner is at Niagara Falls. Departure is via the Vineland region of Niagara Peninsula. Length: 9 hrs. Days: Wed, Aug 10 at 2:30 pm ONLY. Cost/person $20.20.

TOUR G—STRATFORD FESTIVAL THEATRE—The drive to Stratford, Ontario takes 2 hrs during which time a packed luncheon will be served. Upon arrival at Stratford Shakespearean Festival Theatre, a matinee performance (cost of ticket included) will commence, after which, time can be spent wandering about Stratford. Length: 5½ hrs. Days: Wed, Aug 10 at 2:30 pm ONLY. Cost/person $19.

THINGS TO SEE

CASA LOMA, 1 Austin Terrace (Spadina, south of St Clair Ave W). A fairytale 98-room castle complete with turrets, secret underground passages, and a dungeon. Open daily, 10 am-8 pm. Admission: Adults, $2; students and seniors, $1; children, 50¢. (923-1171)

CHINATOWN, Dundas St W at Elizabeth to Dundas W to Spadina. Newest attraction is China Court with authentic pagodas, gardens, and Chinese boutiques.

CITY HALL, Bay & Queen St. Open daily, 10:15 am-5:15 pm. Tours available. (367-7999)

CN TOWER, 301 Front St W (Front & John St). World's tallest free-standing structure which serves as a communications antenna for numerous TV and radio stations features three observation levels, revolving restaurant, and many shops. Open, Mon-Fri, 10 am-11 pm; Sat & Sun, 9:30 am-11 pm. Admission to observation levels: Adults, $2.75; seniors and students, $2.25; children, $1.50. (360-8500)

FORT YORK, Garrison Rd (entrance off Fleet St). Restored military fort of the War of 1812. Open Mon-Sat, 9:30 am-5 pm; Sun & holidays, noon-5 pm. Admission: Adults, $1.00; children and seniors, 25¢. Family rate, $2.50.

HOCKEY HALL OF FAME; SPORTS HALL OF FAME, Exhibition Place. Historic memorabilia, photos, and artifacts of NHL and other sports events. Open 10:30 am-8:30 pm, Tues-Sun. Admission: free. [595-1345 (hockey); 366-7551 (sports)]

KENSINGTON MARKET, Spadina Ave and Augusta vicinity. A babel of tongues can be heard and a profusion of exotic foods can be bought among kosher butcher shops, Portuguese fresh fish stores, bakeries, West Indian fruit stands, and cluttered antique shops.

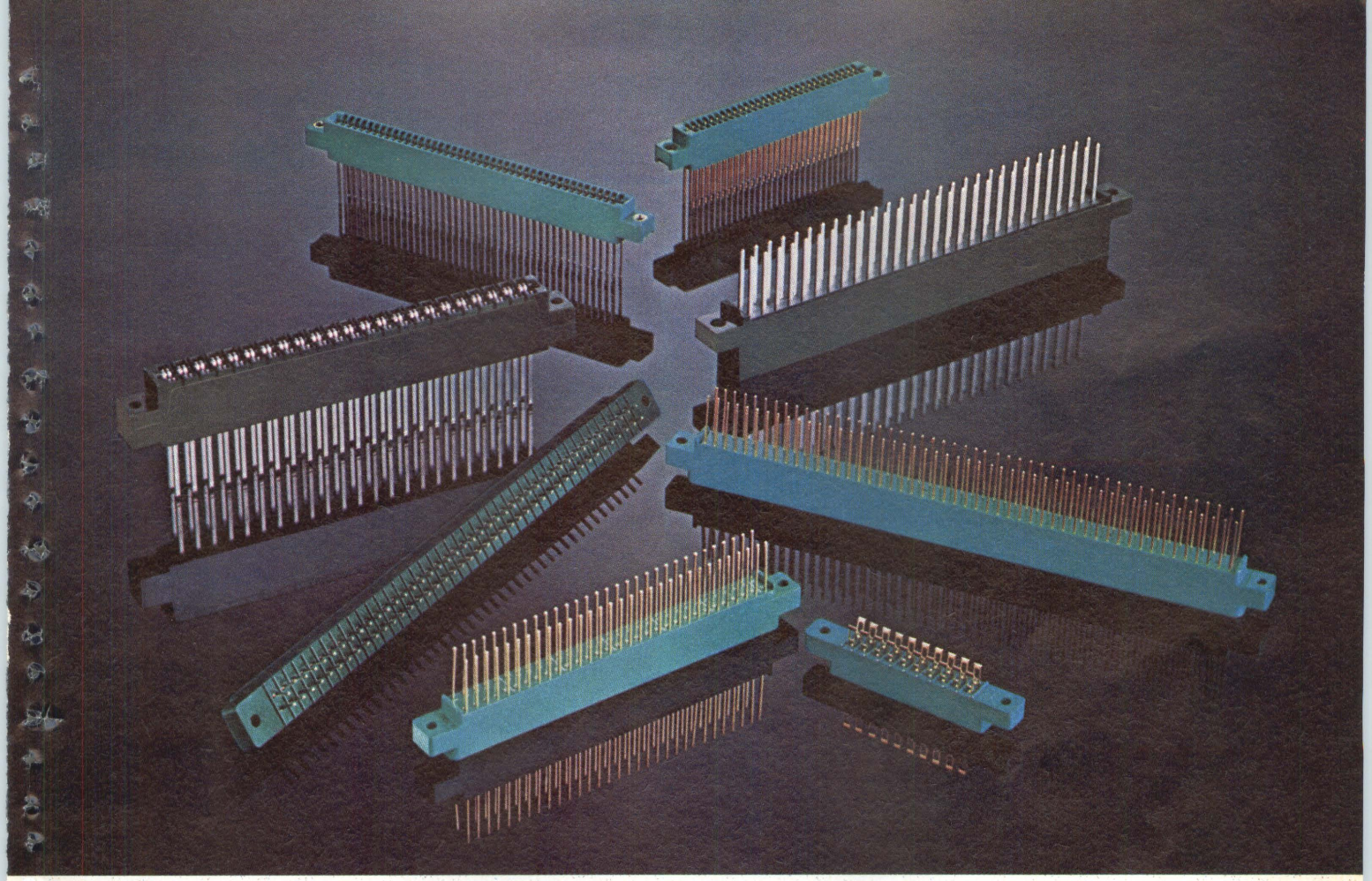
METRO TORONTO ZOO, Meadowvale Rd. New 710-acre zoo is based on the principle that animals are most comfortable in their natural surroundings. Admission: Adults, $3; teens and seniors, $1.50; children, 50¢. (284-0123)

O'KEEFE CENTRE FOR PERFORMING ARTS, Front & Yonge St. Home of the Canadian Opera Co and the National Ballet of Canada. See daily newspaper for current attractions. (366-8484)

OLD TOWN, bound by King St on the north, Front St on the south, Sherbourn on the east, and Yonge on the west. This section, restored to its original elegance, is the home of many shops and restaurants.

ONTARIO SCIENCE CENTRE, 770 Don Mills Rd. Exhibits, demonstrations, workshops, film, and mini-theatres invite involvement, fun, and discovery. Open daily, 10 am-6 pm. Admission: Adults, $1.50; students, 75¢; seniors, 50¢; children, 25¢. (429-4100)

PARLIAMENT BUILDING, Queen's Park. Old Victorian pink-stoned pile, full of marbled corridors, built between 1886-1893, is the home of the Provincial Legislature. Open 8 am-4:30 pm, weekdays. Tours from 9 am-3:30 pm every ½ hr except when Legislature is in session. Confirm in advance. (965-4028)



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We can give you the edge with fast delivery and wide variety in off-the-shelf PC connectors.

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You can also pick the contact you want —gold-dot or gold-plated. These include bifurcated bellows, cantilever beam and bifurcated cantilever beam designs.

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All have been designed to meet the applicable performance requirements of MIL-C-21097, and they're all available now.

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GTE SYLVANIA

CIRCLE 42 ON INQUIRY CARD

IFIP CONGRESS 77 CONFERENCE AT A GLANCE

MONDAY		TUESDAY		
13:30 - 15:00	*15:30 - 17:00*	*8:30 - 10:00*	*10:30 - 12:00*	*13:30 - 15:00*
Future Directions in Computer Architecture *13A*	Education in Computing (1) *14A*	Future Directions in Information Management *21A*	Data Base Organization (Panel) *22A*	Effects of Information Technology on Organization Structures (Symposium) *23A*
Programs of Data Management and Teleprocessing in Larger Organizations (Symposium) *13B*	The Impact of Microcomputers on Computing (Panel) *14B*	Programming Languages *21B*	Computer-Aided Instruction *22B*	Trends and Developments in CAD *23B*
Software Studies (1) *13C*	Programming Management (Panel) *14C*	Data Base Theory *21C*	Impact of Information Systems on Organizations (1) *22C*	Technological Aspects of CAI (Panel) *23C*
Pattern Recognition and Artificial Intelligence *13D*	Theories of Programs and Languages *14D*	Distributed Processing *21D*	Modeling and Analysis of Data Networks *22D*	Foundations for Proofs About Programs *23D*
Communication With Naive Computer Users (Panel) *13E*	New Methods for Information Systems Development *14E*	Graphics *21E*	Which Way in Computer Graphics? (Panel) *22E*	Software Studies (2) *23E*
	Finite Elements Methods *14F*	Numerical Analysis *21F*	Pattern Recognition and Process Control *22F*	Routing and Congestion Control in Switched Data Networks *23F*

	WEDNESDAY			
15:30 - 17:00	*8:30 - 10:00*	*10:30 - 12:00*	*13:30 - 15:00*	*15:30 - 17:00*
Future of Data Management 24A	Data Base Studies (1) 31A	Data Base Studies (2) 32A	Organizational Productivity: The Role of Information Technology (Symposium) 33A	Software Reliability (Panel) 34A
Program Specifications (Panel) 24B	Fault Tolerance 31B	Data Networks: Past, Present, and Future 32B	Packet Networks: Issues, Experiences, Choices 33B	Future Potentials in Computer Communication 34B
Computer-Assisted Training 24C	Distributed Data Switching 31C	Impact of Computerization on Work Content and Job Satisfaction (Panel) 32C	Computer Systems for Education in Universities (Panel) 33C	Very Large Memories (Panel) 34C
Mathematical Theory of Data-Flow Analysis (Panel) 24D		Safer Use of Computers (Panel) 32D	Understanding Natural Languages (Panel) 33D	The Use and Benefit of Formal Description Techniques (Report of Working Group 2.2) 34D
Process Control 24E	Telecommunications Management (Symposium) 31E	Performance Evaluation 32E	Program Translation 33E	System Performance 34E
Techniques in CAD (1) 24F		Computational Algorithms 32F	The Impact of Computerization on Leisure Activities 33F	Is the Erosion of Privacy an Unavoidable Consequence of Computer Applications? (Panel) 34F

THURSDAY				
8:30 - 10:00	*10:30 - 12:00*	*13:30 - 15:00*	*15:30 - 17:00*	*8:30 - 10:00*
Programming Support Systems *41A*	Graphics in Software Engineering *42A*	Electronic Mail (1): Design (Panel) *43A*	Electronic Mail (2): User Needs (Panel) *44A*	Operating Systems *51A*
Data Bases Business Systems and Privacy *41B*	Interactive Approaches to Corporate Planning and Control (Symposium) *42B*	CAD: Perspectives and Prospects *43B*	Cost Benefits of Computer Services (Panel) *44B*	The Impact of Computerization on Employment (Panel) *51B*
Education in Computing (2) *41C*	Hardware Aids to Software *42C*	Decision Support Systems *43C*	Automated Design in Electronics *44C*	Software Engineering Education (Panel) *51C*
Specification and Verification of Communication Protocols (Panel) *41D*		Logic and Proofs for Programs *43D*	Verification and Programming *44D*	Complexity Theory *51D*
Soft Hardware *41E*	Computerized Evaluation and Computational Learning *42E*	A Philosophy of Teaching Computing Science the World Over (Panel) *43E*	Impact of Information Systems on Organizations (2) *44E*	Parallel Architectures *51E*
	Specialized Computer Services *42F*	System Programming *43F*	Models of Environment (Panel) *44F*	

FRIDAY				
10:30 - 12:00	*13:30 - 15:00*	*15:30 - 17:00*		
Programming Methodology *52A*				
The Social Accountability of Computing (Panel) *52B*	New Approaches to Systems Integrity *53B*	Distributed Systems: Operational and Privacy Requirements *54B*		
Computer Education for Two-Year Colleges and High Schools (Panel) *52C*	Numerical Methods in Mathematical Physics and in Control Theory *53C*	Programming Systems *54C*		
Systems for Public Planning and Control *52D*	Formal Theories of Programs and Parallelism *53D*	Concepts in Parallel Programs *54D*		
Techniques in CAD (2) *52E*	Design Automation for LSI-- Practical or Painful? (Panel) *53E*	Economics, Organizational, and Social Implications of CAD (Panel) *54E*		

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THE WORLD'S FIRST 4K STATIC BIPOLAR RAM IS READY FOR ACTIVE DUTY.

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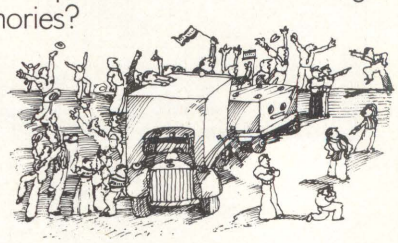
Fairchild proudly introduces the very first, fully static, 4K Bipolar TTL RAM.

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What else would you expect from the world's largest supplier of Bipolar Memories?

FASTER THAN A ROLLING MOS.



If you think that MOS memories roll along at a pretty fast clip, wait till you see our new static Bipolar RAM perform. The new Fairchild 93471 has an incredible T_{AA} of 50ns max, and 25-30ns typical. On top of all that speed, you get Bipolar reliability backed by Fairchild's Walled Emitter Isoplanar™ process.

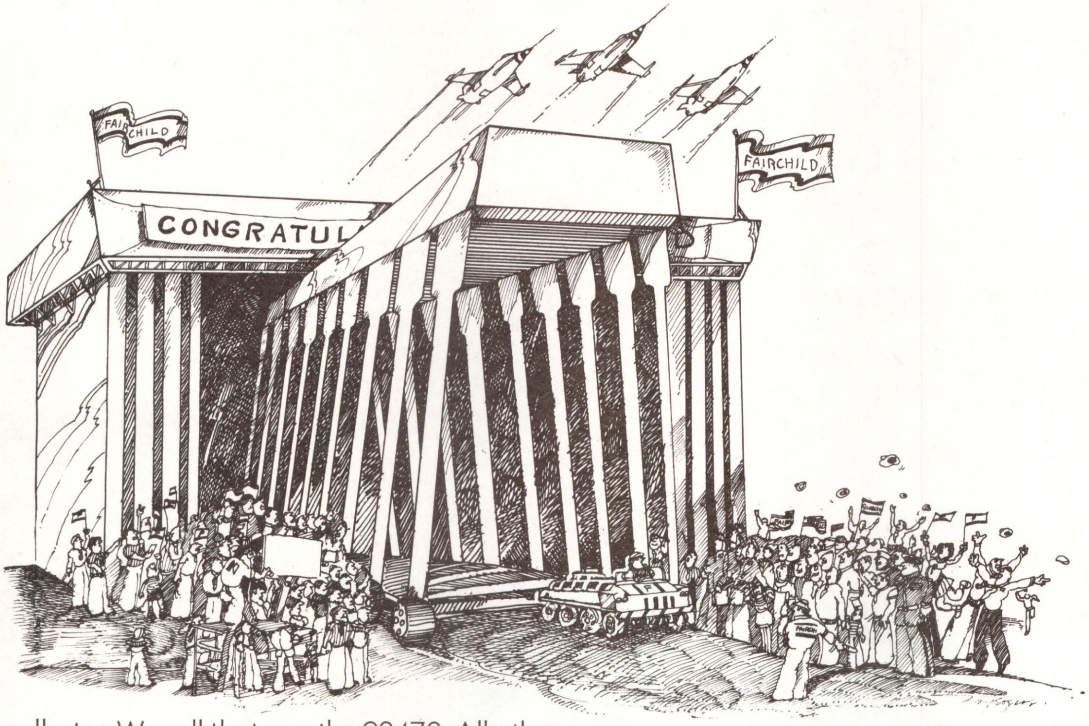
Also, because our new device is fully static, no special clocking or refresh circuits are required.

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The new 93471 is organized 4096 by one bit. It's a 3-state device in an 18-pin package. It offers full decoding on the chip, separate data input and data output lines, and active LOW chip select lines.

The power supply is 5 volts with power dissipation 0.12 mW/bit typical. You also get operation over full military and commercial temperature ranges.

The 93471 also comes in a version with an open



collector. We call that one the 93470. All other specs are the same.

RAM OF MANY TALENTS.

The new Fairchild 4K RAM is ideal for mainframe memories, controllers, minicomputers, CRT terminals, peripherals, add-on memories and a great number of military applications. Circuitry uses include cache, buffer and scratch pad memories.

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Your Fairchild distributor, sales office or representative can get you all the parts and specs you need to completely fall in love with our new 4K RAMs. For more immediate results, call the direct line at the bottom of this ad. Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, California 94042. Telephone: (415) 962-3951. TWX: 910-373-1227.

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NCR's new, fast, portable, bi-synch terminal em-t5

NCR's new portable bi-synchronous KSR terminal communicates at 2400 BAUD with an IBM 3270 (EBCDIC) data based system operating in a poll/select mode.

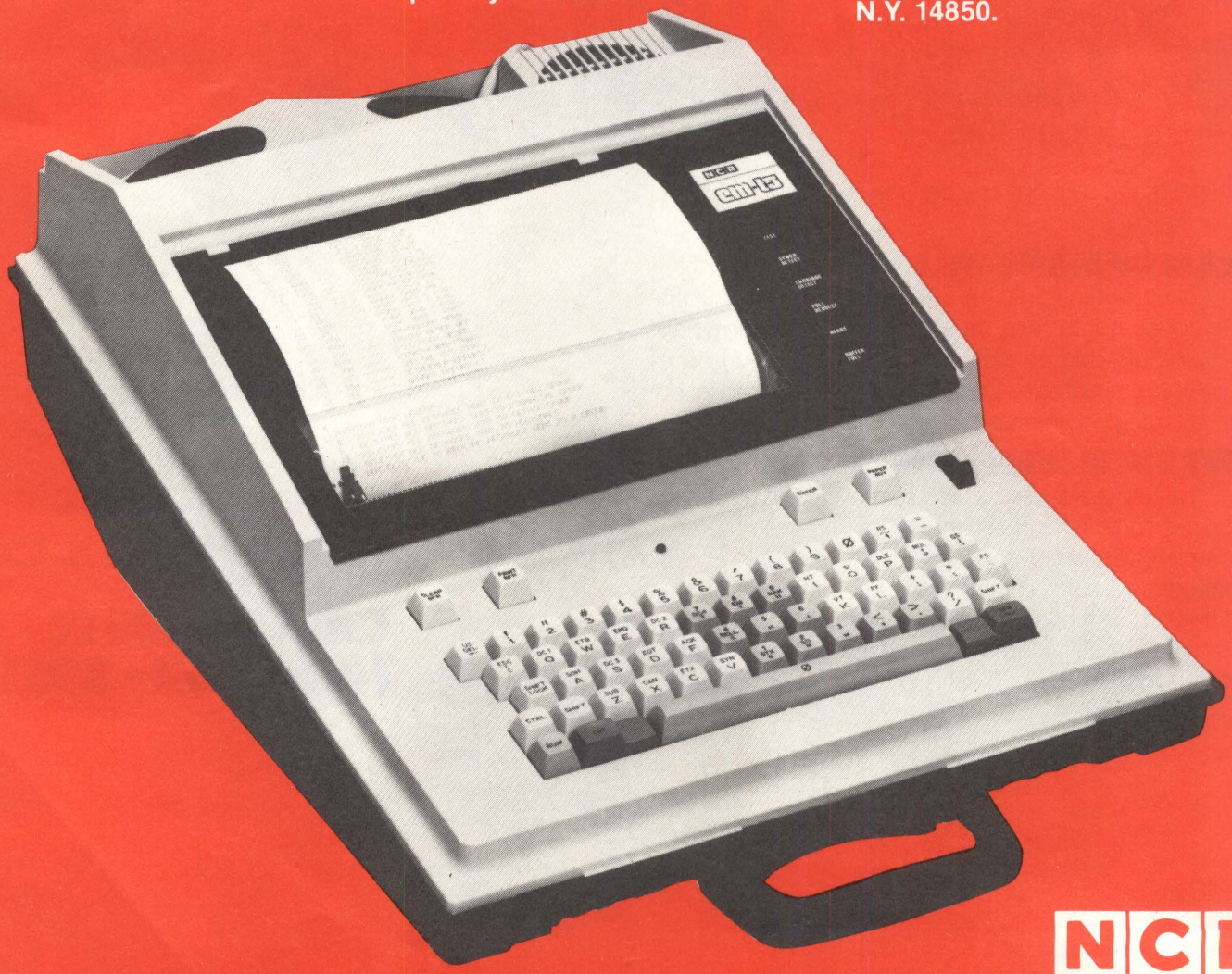
The 2000 character buffer permits communications at 2400 Baud with the computer. To transmit, inquiries are typed into the memory and held until polled by the computer, then transmitted at 2400 Baud. Requested information is transmitted back from a data based system at 2400 into the terminal memory. It is then printed out at 30 CPS. This greatly reduces the computer "On-Line" (connect) time.

The terminal will have some edit capability while entering a message into memory and a capability for additional copies.

Incoming messages will have priority and be received into memory, except when the terminal is in the transmit mode (awaiting to be polled), or when the memory is full.

Messages will be printed out as soon as an (EOT) control signal is received into memory and the cyclic redundancy code (CRC) character is verified. Messages will remain in memory until replaced by another message or until the "clear-memory" button is activated.

To communicate with a computer, all that is needed is an electric outlet and a telephone jack. Set-up time takes only seconds. For immediate action, phone John Petry, Director of Marketing, at (607) 273-5310 or write Terminal Systems Division — Ithaca, P.O. Box 627, Ithaca, N.Y. 14850.



NCR

Terminal Systems Division — Ithaca

CIRCLE 44 ON INQUIRY CARD

Single-board microcomputers offer hardware cost-effectiveness for implementing many real-time systems. A compatible, resident, real-time executive program provides savings in software development

An Integral Real-Time Executive For Microcomputers

Kenneth Burgett and Edward F. O'Neil

Intel Corporation
Santa Clara, California

Single-board computers, or microcomputers, that contain central processor, read-write and programmable read-only memory, real-time clock, interrupts, and serial and parallel input/output all on one printed circuit board, have made feasible a whole spectrum of applications which previously could not be economically justified. These microcomputers have also opened up a range of applications where the high functional density of large-scale integration provides advantages over previous solutions such as hardwired logic or relatively expensive minicomputers. While microcomputers readily solve hardware requirements, software for single-board computer applications with real-time characteristics (which are in the majority) has until now been generated individually for each application.

The Intel RMX/80* Real-Time Multi-Tasking Executive simplifies real-time application software development, and at the same time furnishes capabilities optimized for the microcomputer environment. It provides the means to concurrently monitor and control multiple external events that occur asynchronously in real-time. The program framework allows system builders to immediately implement software for their particular applications, and to avoid specific details of system interaction.

Major functions of the executive include system resource access based on task priority, intertask communication, interrupt driven device control, real-time clock control, and interrupt handling. In combination, these functions eliminate the need to implement detailed real-time coordination for specific applications.

Previously, two alternative software approaches were used to solve microcomputer applications. First, many designers created their own operating executive, individually tailored for each application. Obviously, this approach was expensive and time-consuming. The second approach was to use a minicomputer executive which had been adapted to a microcomputer. Since this software was designed for a different processing environment and then "stripped down," it suffered from major inadequacies when executed on microcomputers. The alternative, RMX/80, has been designed specifically to provide a general-purpose real-time executive tailored to Intel SBC 80 and System 80 microcomputers.

Real-Time System Requirements

All software design approaches for use in real-time applications include capability for concurrence, priority, and synchronization/communication.

Concurrence—Real-time systems monitor and control events which are occurring asynchronously in the physical world. Microcomputer software does not know exactly when external events will occur; however, it must be prepared to perform the necessary processing upon demand, whenever the events actually do occur. Typically, interrupts are used to inform the microcomputer that an event has occurred. At interrupt time, system control software determines what processing to perform, as well as the relative sequence in which processing must take place.

*RMX/80™ is a registered trademark of the Intel Corp, Santa Clara, Calif.

Programs related to external events are processed in an interleaved manner based on interrupt occurrence and priority. For instance, one routine is executing when an interrupt activates, signaling that a higher priority event has occurred. At this point, the routine related to the priority interrupt is started, while execution of the less important routine is discontinued temporarily. When the more important routine is completed, or temporarily halted for some other reason, execution of the less important routine is resumed. In this manner, multiple programs execute concurrently in an interleaved fashion.

Priority—In a real-time environment, certain events require more immediate attention than others because of their significance within the physical world. Immediacy is relative to other processing, and is determined by application requirements. The concept of immediacy or priority, however, is common throughout all real-time microcomputer applications. In priority-based systems, the most important program (one that is not waiting for some physical or logical reason) is the one executing.

A classic illustration of program priority in real-time systems is found in the area of plant control. When the plant begins to fail in a nonrecoverable manner, it is imperative that the plant be shut down as quickly as possible. For this reason, shutdown processing takes priority over all other system demands. Software priority enforces this hardware concept of physical operational events.

Synchronization/Communication—Another common similarity in most real-time systems is the need for synchronization between various events in the physical world which are under microcomputer control. Synchronization is defined as the process whereby one event may cause one or more other events to occur. Communication is the process through which data are sent between input/output (I/O) devices or programs and other programs within the microcomputer system.

An example of the need for synchronization and communication is a microcomputer system for weighing and stamping packages. One part of the system weighs the package, calculates pricing, and releases the package onto a conveyor belt. Price and weight data are communicated to another part of the system which stamps the data onto the package after it arrives at a sensor station. Synchronization is demonstrated by the occurrence of one event—package arrival—causing another event—package stamping—to occur.

Compatible Benefits

To satisfy real-time microcomputer software requirements, the RMX/80 Real-Time Executive software (Fig 1) was designed. This program differs from existing software systems by offering capabilities directly related to the single-board microcomputer environment in which it operates. These capabilities have two major bottom-line benefits compared with equivalent minicomputer systems. First, the executive code is compact enough to allow a large number of real-time applications to be processed on a single microcomputer board. To accomplish this capability, its nucleus is optimized to reside in less than 2k bytes [ie, in a single 16k programmable read-only memory (p/ROM)], thereby allowing up to 10K of onboard memory for application-related software and storage.

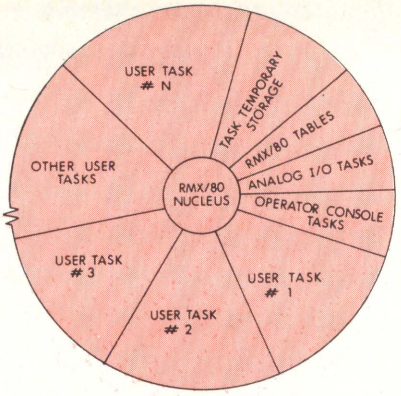


Fig 1 A typical RMX/80 system. Multiple tasks control a given application. Nucleus controls execution of both user and executive tasks through task-to-task communication, real-time clock, priority resolution, and interrupt handling facilities. All tasks within an RMX/80-based application use at least some of these capabilities; other optional executive tasks include debugger, free-space manager, and device control for operator's console, diskette file system, analog subsystems, and high speed mathematics unit

Second, the executive may be p/ROM-resident. When the microcomputer system is powered on, the software system (executive plus application programs) is automatically initialized and begins execution of the highest priority application task. Typical major real-time executives, however, are totally random-access read-write semiconductor memory (RAM)-resident, which means they must be initialized (booted) from a peripheral device, such as diskette, cassette, or communications line, into microcomputer memory. The need for peripheral devices significantly increases the total cost of traditional real-time executive-based solutions.

Sample Application

Functioning as a real-time executive for microcomputers, this software system provides facilities for orderly control and monitoring of asynchronously occurring external events. Although these events may differ widely from application to application, facilities are adaptable to nearly all processes where the microcomputers are used, including process and machine control, test and measurement, data communications, and specialized online data processing applications (where one or more terminals access diskette-based data). The executive is particularly useful in dedicated low cost applications which were not economically feasible before the advent of microcomputers. For example, consider the requirement of gas pump control in a service station (Fig 2).

In this station, a microcomputer system operating with RMX/80 concurrently monitors and controls multiple gas pumps, and sends price and volume informa-

tion to one central location. At the same time, information about station operation is being transmitted over a communications line to a regional computer.

Individual tasks are developed independently to measure gas flow, calculate and display price information, transfer data to the central computer, and monitor levels of gasoline in underground storage. All this processing takes place concurrently under program control. (Credit verification, charge slip printing, and billing can also be controlled by additional software tasks.)

Efficient gas station operation demands that the hardware/software system be highly reliable. The compatible benefits of compact code, p/ROM residency, and self-initialization on a single-board microcomputer system all combine to ensure functional integrity.

Software Structure

RMX/80 simplifies the effort for developing a real-time system, first, by providing many commonly required software functions. Second, its software structure promotes efficient program development. Programmers who are familiar with structured programming will find task orientation both natural and easy to use.

Tasking means that a larger program is divided into a number of smaller, logically independent programs or tasks. The key is to identify functions that may occur concurrently. For example, consider the tasks required for a terminal handler—real-time asynchronous I/O between an operator's CRT terminal and the executive.

Input Handler Task—One task must be ready to accept a data character from the terminal at any time. This is done by responding to an interrupt signal from the terminal and then accepting the data character. The task immediately passes the input character to a subsequent task automatically and then goes back to wait for another interrupt.

Line Buffer Task—As characters are received from the input handler they must be placed into a buffer to form a line. Eventually, the buffer will be filled or the logical end-of-line will be signaled by a carriage return character. At this point, the line buffer must be sent to some other task for processing.

Echo Driver Task—For a full-duplex terminal, it is necessary to return each input character to the terminal for display on the CRT screen. This task waits for a character, which could be sent by either the line buffer or input handler task, and then sends the character to the terminal. It then waits for the next character.

Note that input handler and echo driver are described as waiting for an event. Within the RMX/80, that is literally the case. While they wait, however, system resources are available for other tasks, such as that of the line buffer. Thus, effective processing may occur concurrently with necessary waiting periods. Notice also that a number of other tasks may also be active within the system. In fact, the greater the number of tasks running concurrently, the more effectively system resources are used. Concurrent operation eliminates many time wasting procedures from a real-time system. For example, the executive can eliminate the need for many timing loops where the processor simply executes a no-operation instruction repeatedly while waiting for an event to occur.

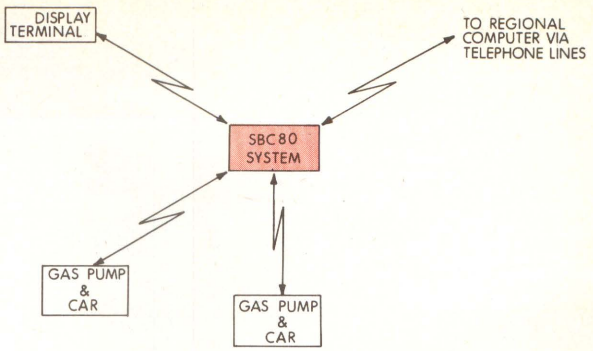


Fig 2 Microcomputer control for gas pump automation. In this example, executive-based system simultaneously controls two pumps, displays information on operator's console, and communicates with regional computer. At a given time, more or fewer functions could be operating concurrently. System expansion can be easily accomplished by adding tasks and modular hardware

Within the executive, tasks not only are logically independent, they are also physically independent, actually contending with each other for the use of the processor and other system resources. The executive resolves this contention based on the priority of each task.

In the terminal handler example, it is clear that the input handler must have highest priority, since acceptable performance cannot tolerate the loss of data. Second highest priority is given to the echo driver, so that data appearing on the screen remain coordinated with the input. Lowest priority goes to the line buffer, since that function does not depend directly on an external asynchronous event. There are no particular real-time constraints on the line buffer as long as the input characters are eventually processed.

It is possible to write the entire terminal handler as a single large task instead of as several smaller tasks. However, consideration must be given other high priority tasks operating within the system which may not be able to gain control while a low priority portion of the terminal handler, such as the line buffer task, is executing. Therefore, tasks assigned as high priority are generally kept as short as possible. If the terminal handler were written as one large task, it could tie up the entire processing system for a relatively trivial function.

Task States

Two task states have been implied—running and waiting. A running task is always the task which currently has the highest priority and is not suspended or waiting. A waiting task remains in the wait state until it receives a message or an interrupt for which it is waiting or until a specified time period has passed. The wait period can be timed using the system clock.

A running task may suspend itself on some other task in the system. A suspended task cannot begin execution again until some running task orders it to resume. As an example, a password routine might temporarily suspend the echo driver of the terminal handler so that the password is not displayed. (The password routine must

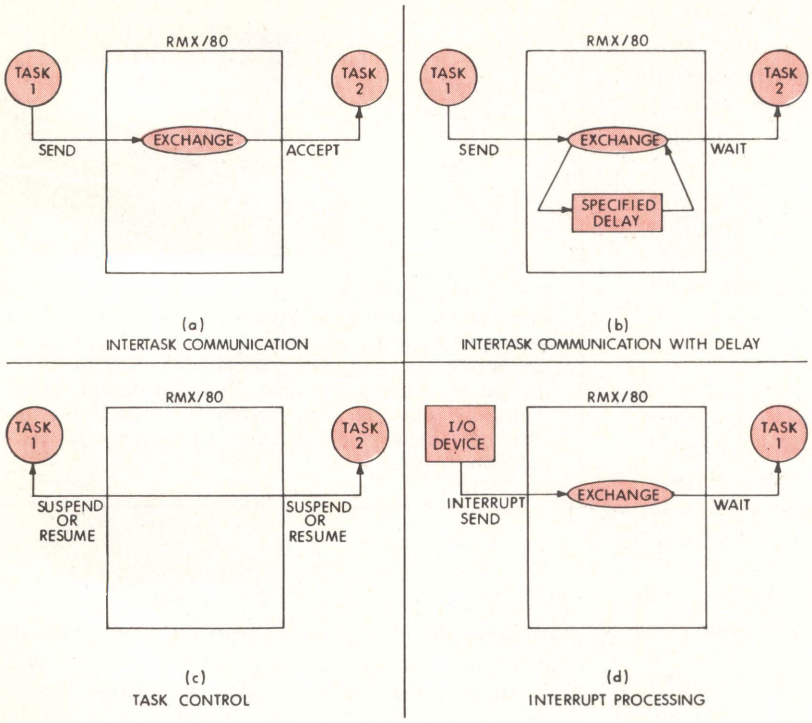


Fig 3 System message exchanges. In intertask communication (a) task 1 sends a message to an exchange, where it is held until task 2 requests message via accept. In intertask communication with delay (b), task 2 waits for a message from task 1 until data are available or until a certain time period has passed, whichever occurs first. In task control (c), any task may suspend or resume any other task. In interrupt processing (d), an I/O interrupt is transformed into a message that task 1 receives via a wait command. Task 1 then performs appropriate interrupt processing

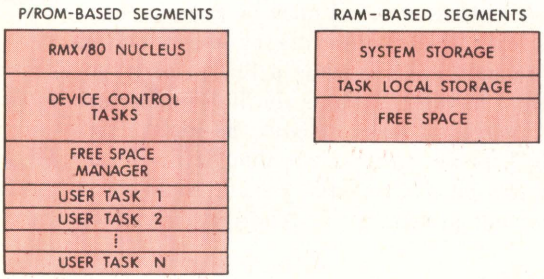


Fig 4 Memory utilization. RMX/80 nucleus, device control task, and free-space allocation modules are linked with user tasks to form a real-time system. Although executive may be RAM-resident, it is designed to reside in p/ROM and uses RAM only for temporary storage and free space. User tasks are provided by user at generation time. RAM may be used by RMX/80 and all associated tasks for temporary storage, including stack

remove the password from the line buffer, or it will be displayed as soon as execution of the echo driver is resumed.)

A task may also be in the ready state. A ready task is one that would be running except that a task with higher priority temporarily controls the system resources. The executive maintains a list of all tasks that are ready to run. The next task to be run is always the task with the highest priority in the ready list.

The running task relinquishes its control of the system by

(1) Putting itself into a wait state

(2) Suspending itself

(3) Sending a message to a higher priority task, which if it has the highest current priority, becomes the running task

(4) Being preempted by an interrupt to a higher priority task

In the case of an interrupt, the executive saves the status (contents of registers, etc) of the interrupted task so that it will be restarted correctly.

Message Exchanges

Tasks communicate with each other by sending messages (Fig 3). The sending task constructs the message to be sent in RAM or uses a previously assembled message.

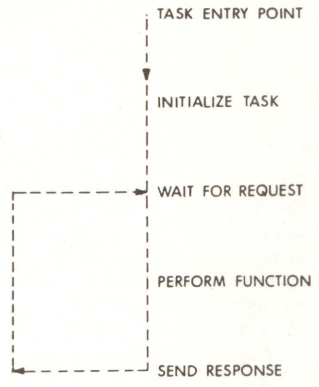


Fig 5 Consumer task flow. Consumer task performs initialization and then drops into cyclic loop, alternately waiting for messages, performing functions requested by message, and sending an acknowledgement in form of a response message

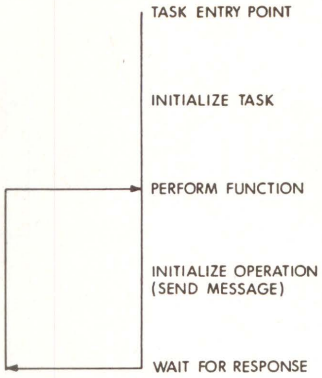


Fig 6 Producer task flow. Producer processing flow is opposite to that of consumer task. Instead of passively reacting to requests from other tasks, producer task issues requests to which other tasks must respond

The sending task then issues a SEND command that posts the address of the message at an exchange.

An exchange is simply a set of lists maintained by the executive. The first list contains the addresses of messages available at that exchange. The second list consists of a list of tasks that are waiting for messages at that exchange. When a task enters a wait state, it specifies the exchange where it expects eventually to find a message. The task may wait indefinitely, or it may specify that it will only wait a specific period of time before resuming execution.

Messages, together with the exchange mechanism, provide for automatic intertask communication and also for task synchronization. For example, a message to a particular task may specify that the task is to send a response to a certain exchange. Thus, the original task may request an acknowledgement response to its message, or it may specify that a message is to be sent to a third task. RMX/80 treats interrupts like messages, the only difference being that interrupts have their own set of exchanges.

Note that the sending and receiving of messages classifies tasks into two types—message consumers and message producers. A consumer task waits for a message, performs an action based on the message, and then returns to the wait state until another message is received. A producer task initiates its function by sending a message to another task, waits for a response, and then sends another message. Figs 5 and 6 graphically illustrate the processing within these two tasks. The distinction between consumer and producer tasks is relative since many tasks act as both consumer and producer.

Executive Modules

RMX/80 is supplied as a library of relocatable and linkable modules. These modules are added selectively as required when the user-supplied tasks are passed through the link program. Only modules actually requested by the application are linked in. For example, if the application program does not specify use of the free-space manager, that module is not linked into the system.

One module, the nucleus, provides basic capabilities (concurrence, priority, and synchronization/communication) found in all real-time systems. Additional, optional modules may be configured with user programs (tasks) to form a complete application software system. These modules include:

Terminal handler—Providing real-time asynchronous I/O between an operator's terminal and tasks running under the RMX/80 executive, the handler offers a line-edit feature similar to that of ISIS-II and an additional type-ahead facility. (ISIS-II is the supervisory system used on the Intellec Development System.)

Free-space manager—This module maintains a pool of free RAM and allocates memory out of the pool upon request from a task. In addition, the manager reclaims memory and returns it to the pool when it is no longer needed.

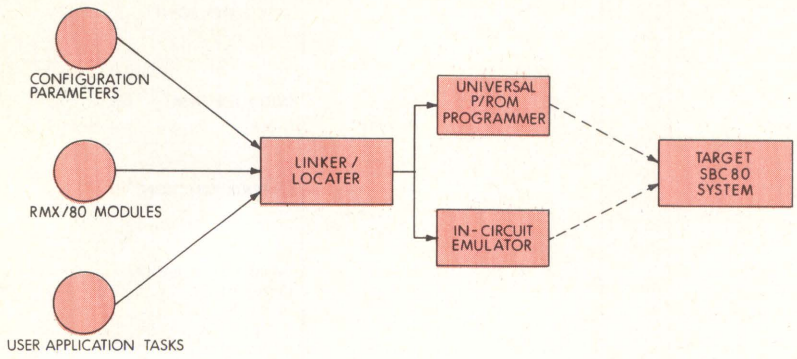


Fig 7 Target microcomputer system. Configuration parameters are linked together with appropriate RMX/80 and user task modules. Resulting program is then transferred to its target SBC 80 system via programmed p/ROMs or is debugged using in-circuit emulation and then transferred

Debugger—Designed specifically for debugging software running under the RMX/80 executive, the debugger is used by linking it to an application program or task. Thus, it can be run directly from the single-board computer's memory. In addition, an in-circuit emulator, such as ICE-80, can be used to load and execute the debugger, providing all resources of the Intellec development system to simplify debugging effort.

Analog interface handlers—Consisting of RMX/80 tasks, these handlers provide real-time control for SBC 711, 724, and 732 systems.

Diskette file systems—Giving RMX/80 users diskette file management capabilities, the diskette driver allows users to load tasks into the system and to create, access, and delete files in a real-time environment without disrupting normal processing. All file formats are compatible with ISIS-II for both single and double density systems.

In addition to application program module or task requirements, the user also supplies a set of generation parameters. These parameters are a set of tables that inform the executive of the number of tasks and exchanges in the system. Fig 7 illustrates the system generation process.

Summary

The significance of RMX/80 to software design parallels the significance of the single-board computer to hardware design. Microcomputers allow designers without extensive experience in digital systems to bring computer processing power into their applications. Similarly, the executive relieves the hardware designer of much software design required for real-time applications. Designed to facilitate growth, since new software needed to support hardware expansions can be supported easily by the addition of new tasks, this executive also substantially reduces recurring costs because it requires a minimum of memory and does not require peripheral bootstrap loading devices. RMX/80 results in economical, shorter, and more flexible software development efforts when designing, building, and verifying real-time user applications.

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Edward O'Neil received a BS degree from Louisiana State University and an MBA degree from California State University. Currently software marketing manager for the single-board computer family at Intel Corp, his background includes design and development of real-time operating systems.

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General-Purpose Registers	16	4	8
Hardware Index Registers	15	2	8
Maximum Memory Available (KB)	64	64	56
Directly Addressable Memory(KB)	64	2	56
Automatic Interrupt Vectoring	Standard	N/A	Standard
Parity	Optional	Optional	N/A
Cycle Time (nanoseconds)	600	800	725

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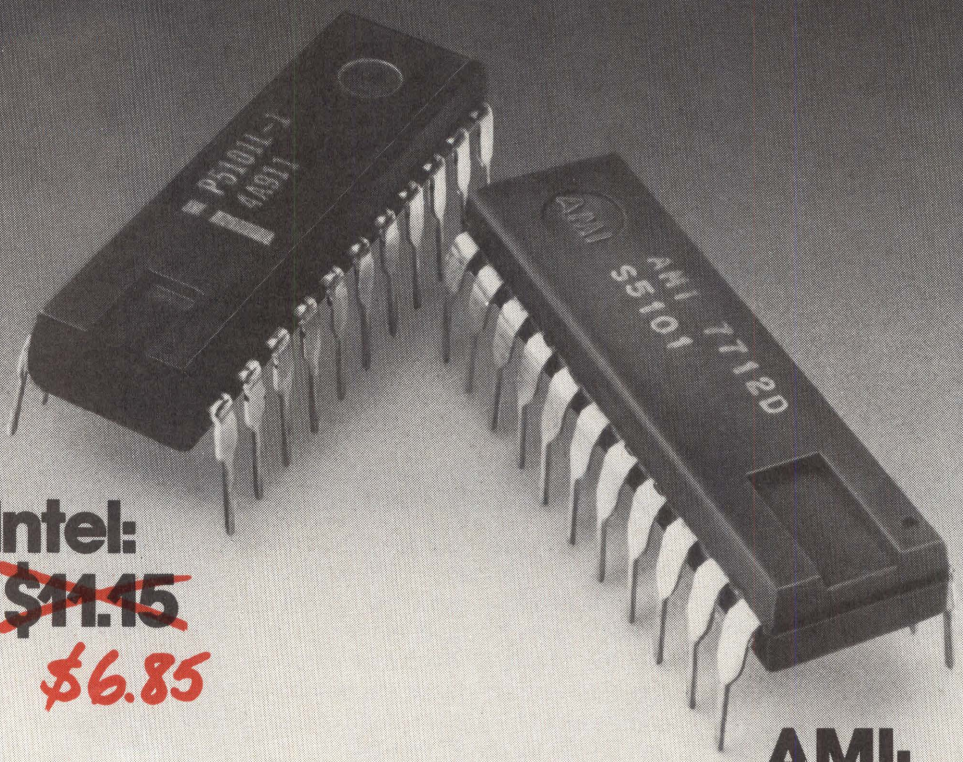
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Interface timing and control of 16-pin 4k and 16k RAMs are more complex than those for the 18- and 22-pin designs. Failure to understand the problems can result in a marginal system design

Timing Peculiarities of Multiplexed RAMs

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Innovative address multiplexing architecture for semiconductor memory is provided by the 16-pin 4k random-access memory, which also offers substantial advantages over 18- and 22-pin devices (Fig 1). Advantages and disadvantages of this architecture have been thoroughly documented (see Bibliography). The major advantages of the 16-pin design are reduced package area, fewer interface drivers required, all transistor-transistor logic interface, and better pinout for more efficient printed circuit board layout. The major disadvantage is a somewhat complex timing cycle involving the six addresses, two clocks, write enable, and data in. Recently, similar random-access memory (RAM) devices with a capacity of 16k bits have been introduced; the timing problems of 4k RAMs also apply to 16k devices.

Evolving into two types with many similarities, 16-pin 4k RAM designs also have some well-defined differences in both logic and timing characteristics. This article clarifies the timing characteristics and highlights the differences between the two RAM design types.

For reference purposes, the early 4k design is designated as the 4096; the later 4k type is referred to as the

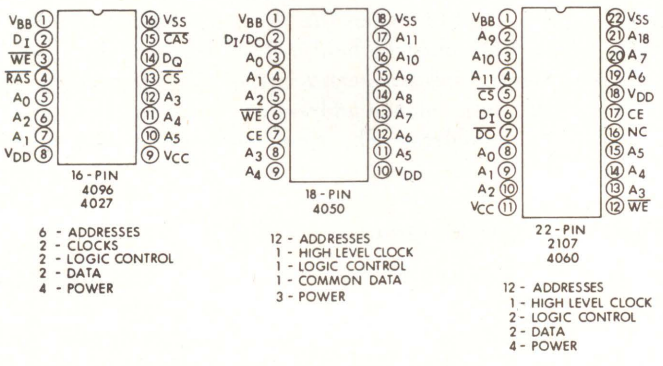


Fig 1 Comparison of package pin connections and logic functions for commonly used 16-, 18-, and 22-pin 4k RAMs

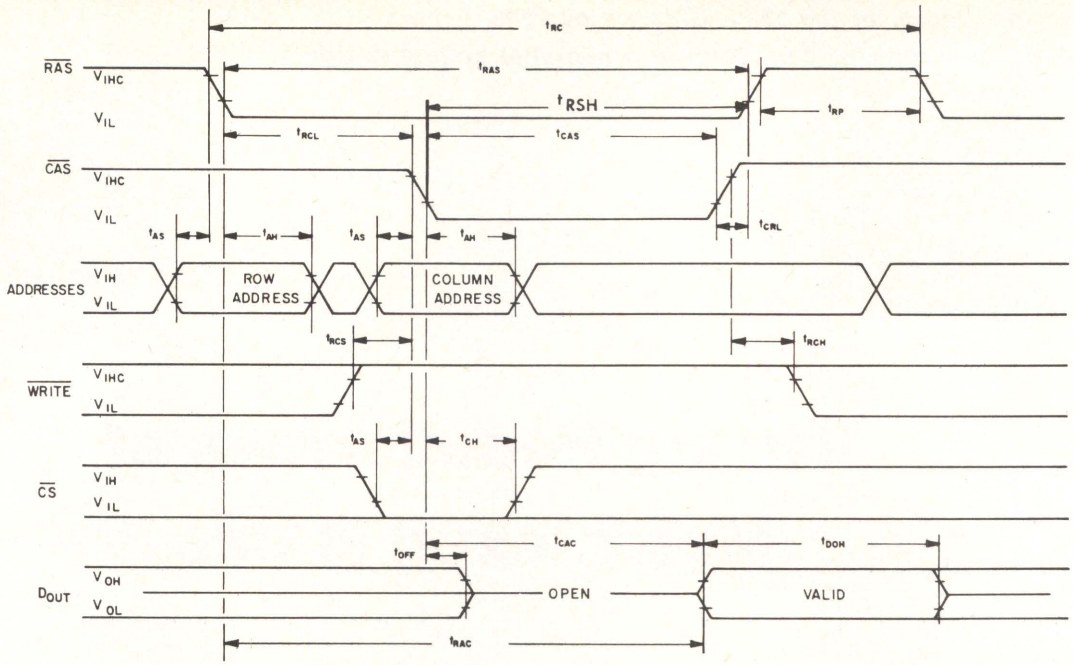


Fig 2 4096 read cycle. X address is set up first. When this address is stable, $\overline{RAS}$ can be turned on. Then address can be changed to Y address. When Y address is stable, $\overline{CAS}$ can be turned on. After t_{CAC}, D_{OUT} changes from a floating state to a stable data out value

4027. A newly introduced 16-pin 16k RAM, defined as the 4116, has timing characteristics similar to those of the more recent 4k design. These numbers refer to the generic device class; many suppliers of these compatible parts use other numbers for their designs.

Interface Signal Definitions

Various timing parameters that must be controlled to ensure proper and/or efficient operation of the memory array are shown on the timing diagrams that are included in the text. Interface signals are defined as follows:

(1) Two clocks, X-clock $\overline{RAS}$ and Y-clock $\overline{CAS}$
(2) Six addresses, A_0 to A_5 (seven addresses on 16k devices)
(3) Write enable, $\overline{WRITE}$ (or $\overline{WE}$)
(4) Data in, D_{IN}
(5) Data out, D_{OUT}
(6) Chip select, $\overline{CS}$ (on 4k only)
(7) Four power pins, V_{DD}, V_{SS}, V_{BB}, and V_{CC}

The sequence of events which must be followed in performing 4096 and 4027 read cycles follows (see Figs 2 and 3).

(a) Set up X address (six signals) and chip select, $\overline{CS}$*
(b) Turn on X clock, $\overline{RAS}$
(c) Wait until X address is captured
(d) Change address signals from X address to Y address
(e) Turn on Y clock, $\overline{CAS}$
(f) Wait for valid data to appear on D_{OUT}
(g) Turn off $\overline{RAS}$ and $\overline{CAS}$
(h) Wait for memory array to precharge in preparation for next cycle

Steps (a) and (b) are straightforward. Step (c) has some complications when the 4027 RAM is considered. Severe complications between RAMs occur with steps (d), (e), and (g), and are discussed in detail; in addition, complications relating to the write cycle are covered.

Initial Portions of Read Cycle

The read cycle starts with setting up the X address. When the address is stable, $\overline{RAS}$ can be started on. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter t_{AS} (t_{ASR} for 4027). Following the time when the clock reaches its true level, the X address must be held stable long enough to be captured. Controlling parameter is t_{AH} (t_{RAH} for 4027). Following this interval, the address can be changed from X address to Y address. The time required to accomplish this is called t_{XY} in some user specifications.

Y Clock Timing

Complications first arise relative to the time at which $\overline{CAS}$ can be turned on. Leading edge of $\overline{CAS}$ is controlled by parameter t_{RCL} for the 4096 and t_{RCD} for the 4027 and 4116. These parameters are essentially the

*Timing of $\overline{CS}$ is non-critical and can occur as late as step (d).

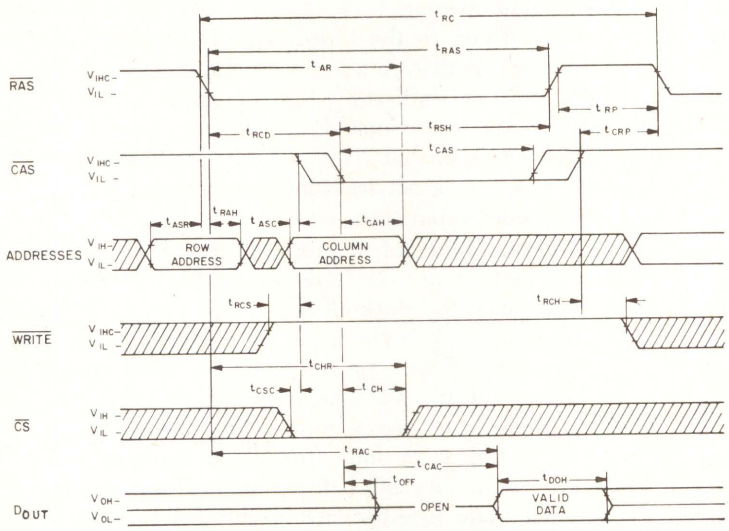


Fig 3 4027 read cycle. X address is set up first. When this address is stable, RAS can be turned on. Then address can be changed to Y address. When Y address is stable, CAS can be turned on. After t_{CAC}, D_{OUT} changes from a floating state to a stable data out value

same, except that t_{RCL} references the beginning of the "on" edge while t_{RCD} references the stable "on" level of CAS.

Data sheets usually give minimum and maximum values for t_{RCL} (t_{RCD} for 4027). Neither value is a fundamental device parameter but is related to actions on other signals.

Basic limit on the CAS leading edge is that CAS cannot start on until the Y address is stable. This is controlled by parameter t_{AS}, which is 0 ns for the 4096. For the 4027, internal delays allow CAS to come on slightly early; thus, the controlling parameter is t_{ASC} and is equal to −10 ns.

An equation for t_{RCL} (min) and t_{RCD} for the 4027 can be set up based on these principles.

4096 $t_{RCL}\ (\text{min}) = t_{AH} + t_{XY} + t_{AS}$

4027 $t_{RCD}\ (\text{min}) = t_{RAH} + t_{XY} + t_{ASC} + t_{TC}$

where t_{TC} = CAS negative transition time

There is no operating maximum on t_{RCL} even though one is usually listed on the data sheets. The value given is more properly called a pseudomaximum value. This results from the internal circuitry of the memory chip. The signal that gates the decoded Y address into the internal data multiplexer is delayed until the sense amplifiers are stable. A "window" exists between the earliest time that the Y address can be set in [see t_{RCL} (min)] and the latest time at which CAS can be turned on without increasing the worst-case data access time. If CAS is turned on at the t_{RCL} (min) time, the Y address is set in early and waits for some time before it is used. In a worst-case part, the Y address is not needed until t_{RCL} (max) time. If CAS comes on later than t_{RCL} (max), the access time will be increased by the time which t_{RCL} exceeds t_{RCL} (max). The relationship between t_{RCL} and access time is shown in Fig 4.

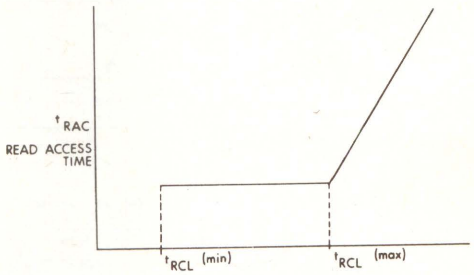


Fig 4 Data access time versus CAS position for worse case part. This diagram shows the effect that a variation in position of CAS-on has on time of valid data out

Note that in a properly functioning RAM, t_{RCL} (max) is *not* an operating limit of the device. Errors will not occur if this value is exceeded, as long as all other parameters are satisfied.

At a time following the turning on of CAS, the data out line changes from a floating state to a stable data

value, representing the data stored in the addressed cell. The parameter that describes this delay is t_{CAC}, which is the delay between either (1) $\overline{CAS}$ actual low or (2) t_{RCL} (max) point, whichever comes last, and stable D_{OUT}. The read access parameter, t_{RAC}, is the time from $\overline{RAS}$-on to valid D_{OUT}. The minimum value is derived as the sum of several other parameters, as follows:

For 4096 $t_{RAC} = t_{RCL}$ (max) $+ t_{CAC} + t_T$

For 4027 $t_{RAC} = t_{RCD}$ (max) $+ t_{CAC}$

Clock-Off Timing

Several constraints influence the off times of the two clocks, $\overline{RAS}$ and $\overline{CAS}$. First is that they must stay on long enough to complete tasks assigned to them. This means that $\overline{RAS}$ must stay on until D_{OUT} has stabilized to valid data (see Figs 2 and 3). In the case of $\overline{CAS}$, this is controlled by parameter t_{CAS}. This is the length of time that $\overline{CAS}$ must be on following the t_{RCL} (max) point in the cycle. (Earlier published data sheets define the parameter t_{CPW} for this function.) t_{CAS} is defined as the $\overline{CAS}$-on duration. This definition is sufficient only when $t_{RCL} \geq t_{RCL}$ (max).

The "off" edge of $\overline{RAS}$ is not clearly defined. In the original 4096 specifications, this edge is defined relative to the $\overline{CAS}$-off edge with parameter t_{CRL}. A typical value for t_{CRL} is about ±50 ns. Exact interpretation of the specifications leads to the conclusion that $\overline{RAS}$ can go off 50 ns before data stabilizes. RAMs are not designed to operate with this timing, even though some will perform without error.

This specification oversight has been corrected by the addition of a new parameter, t_{RSH}, which defines the minimum overlap between $\overline{CAS}$ and $\overline{RAS}$ as the time from $\overline{CAS}$-on to the beginning of $\overline{RAS}$-off. General requirement is that, in addition to the t_{CRL} restriction, $\overline{RAS}$ must stay on until D_{OUT} has stabilized. If either t_{RSH} or t_{CRL} limits are violated, errors can result. The most likely effect is that data will not latch properly. Since the situation is not well defined, the state of D_{OUT} must be considered indeterminate.

Internal logic of the 4027 (and 4116) is different from that of the 4096, causing different constraints to be placed on the clock-off edges. The trailing edge of $\overline{CAS}$ is controlled by parameter t_{CRP}, which is the time between $\overline{CAS}$-off and the next $\overline{RAS}$-on. In published specifications for the 4027, t_{CRP} can go to zero. This means that there is no restriction on the $\overline{CAS}$-off time as long as it remains on long enough to provide valid data (t_{CAS}) and goes off before the next cycle starts. This characteristic is especially useful with the 4116, which does not have a data latch, where it is often necessary to extend $\overline{CAS}$ to hold the data long enough for it to be captured by the system. With the 4027, it simply allows the $\overline{CAS}$-off timing to be non-critical.

Actually, some RAMs are more tolerant. $\overline{CAS}$ can extend into the next cycle but must not go too far into

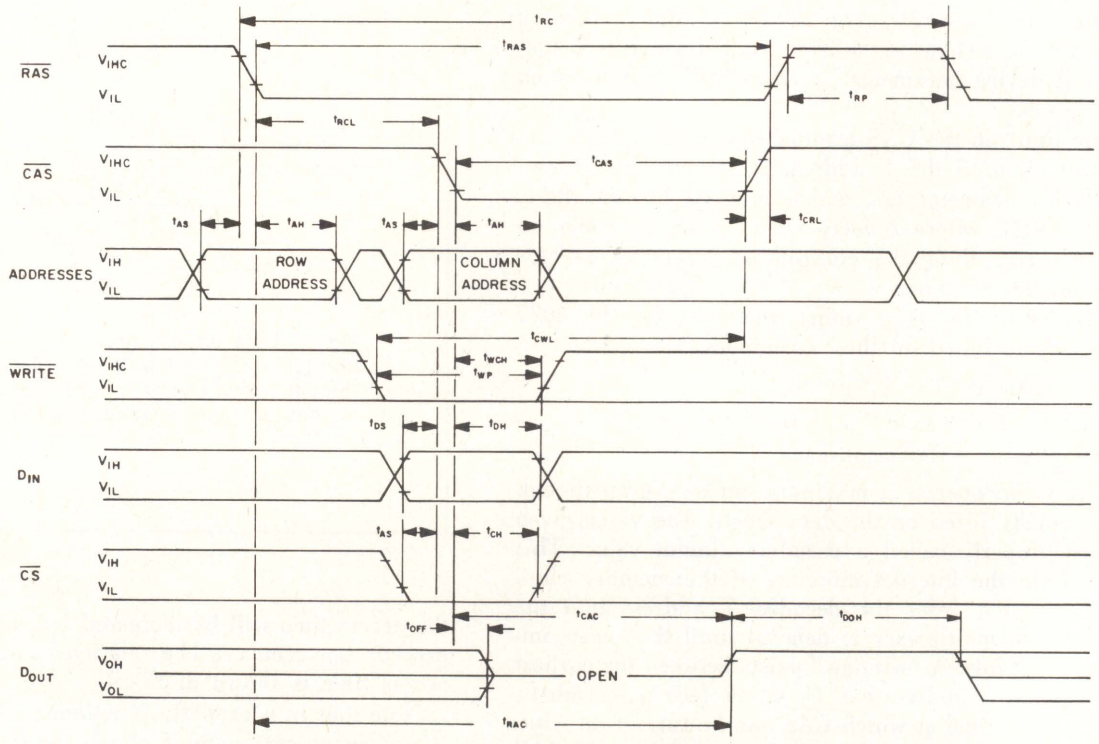


Fig 5 4096 write cycle. Write data are available at the beginning of this "early write" cycle. D_{IN} and $\overline{WRITE}$ are completely noncritical

the t_{RAH} interval of the next cycle; otherwise, the address multiplexing becomes erratic. A reasonable operating limit seems to be on the order of −20 ns for some RAMs; however, this characteristic must be evaluated for each different design since it is not guaranteed by published specifications. This allows the system to use the same timing point to control both timing events, $\overline{RAS}$-on and $\overline{CAS}$-off. Because of the levels used for the definition of t_{CRP}, coincident transitions result in t_{CRP} equal to −10 ns (if t_{TC} = 10 ns). The additional 10 ns is allowed for gate skew.

Unfortunately, this characteristic of the 4027 has not been published; therefore, emulators of the original part may not end up with the same capability. In the meantime, it is feasible to design with t_{CRP} equal to zero.

Limits for $\overline{RAS}$-off are the same for the 4027 and the 4096; controlling parameter is t_{RSH}.

Following the end of $\overline{RAS}$, the only parameter of concern is t_{RP}, the precharge time for circuits controlled by the $\overline{RAS}$ clock. $\overline{RAS}$ must stay off long enough to complete this precharge, at which time, a new cycle can be started. Normally $\overline{CAS}$ is not required to be off for a minimum time, t_{CP}, to precharge circuits, as this function is normally handled by $\overline{RAS}$ when needed. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time. This parameter does not apply during a normal cycle.

In one important respect, the 4116 differs from the 4027; read data are not latched. This means that D_{OUT} is valid only as long as $\overline{CAS}$ remains low. Following the end of $\overline{CAS}$, D_{OUT} will float. The timing freedom of $\overline{CAS}$-off allows data to be held long enough to be captured by the system without extending the cycle time.

Write Cycles

Three different write cycles can be defined from the user's viewpoint: write (W), read-write (RW), and read-modify-write (RMW). From a RAM standpoint, there are actually only two types of cycles: write and read-write. The three user cycles are defined as:

Write cycle—(Figs 5 and 6) Data are available at the beginning of this cycle and the write operation is initiated as early as possible. No read operation is desired.

Read-write cycle—(Figs 7 and 8) Data are read out, but new data to be written are available at the beginning so that the write operation is started as soon as is possible without disrupting the read operation. This can occur before D_{OUT} is stable.

Read-modify-write cycle—(Figs 7 and 8) Data are read out but new data to be written are not available during the read portion. Read data are used in some manner to generate write data. Writing starts as soon as the modify operation is completed and resultant write data are stable. This modify time can range from a few nanoseconds up to many 10s of nanoseconds. The maximum limit on modify time is controlled by the parameter t_{RAS}

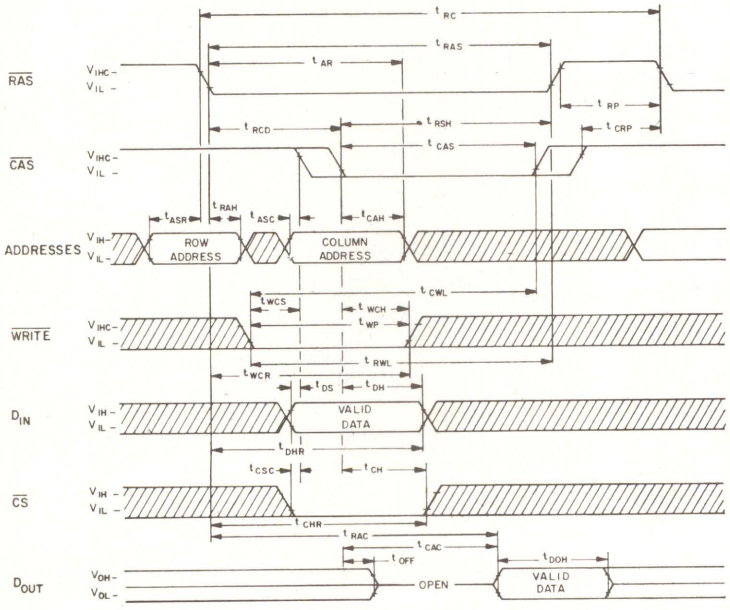


Fig 6 4027 write cycle. Write data are available at the beginning of this "early write" cycle. D_{IN} and $\overline{WRITE}$ are completely noncritical

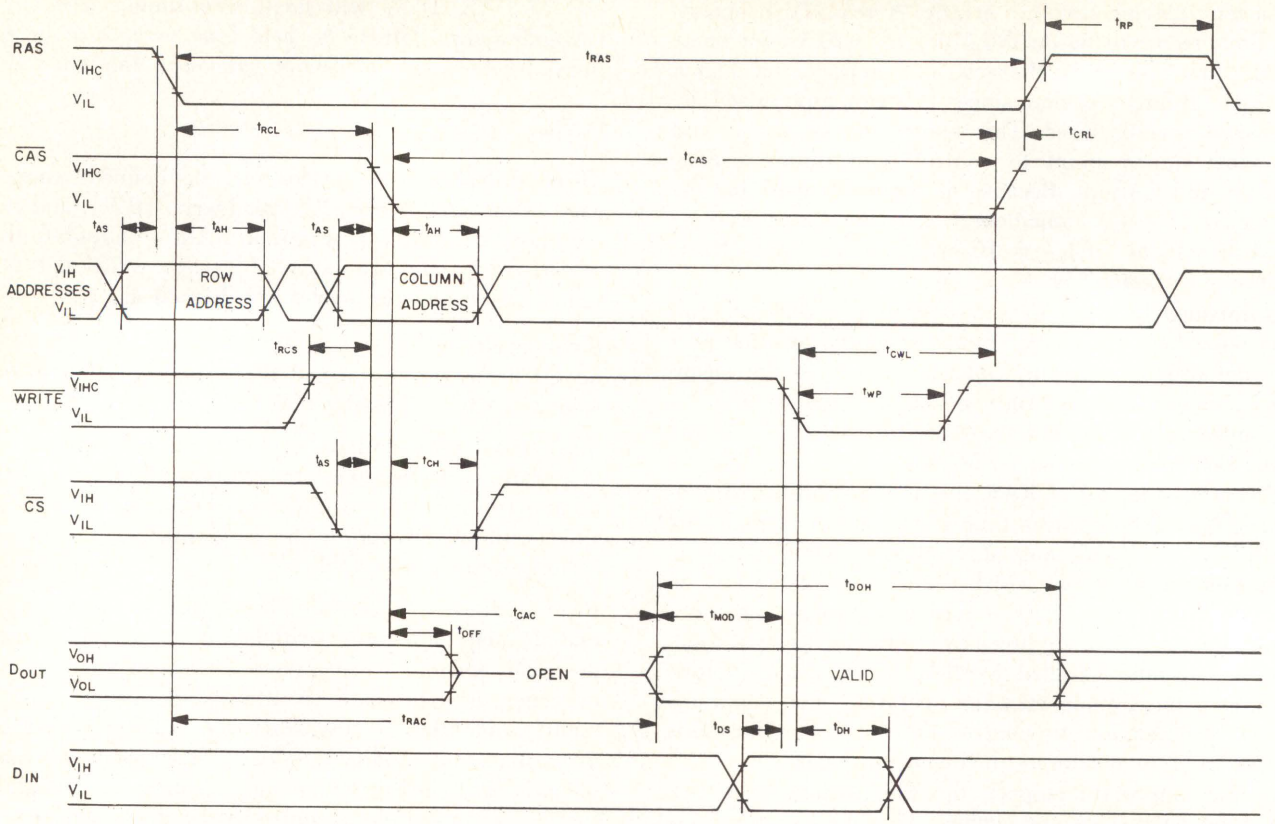


Fig 7 4096 read-write/read-modify-write cycle. This cycle starts as a read cycle, but as soon as characteristics allow, a write cycle is initiated. Write cannot start until after D_{OUT} has stabilized; otherwise D_{OUT} will be disrupted and errors will occur

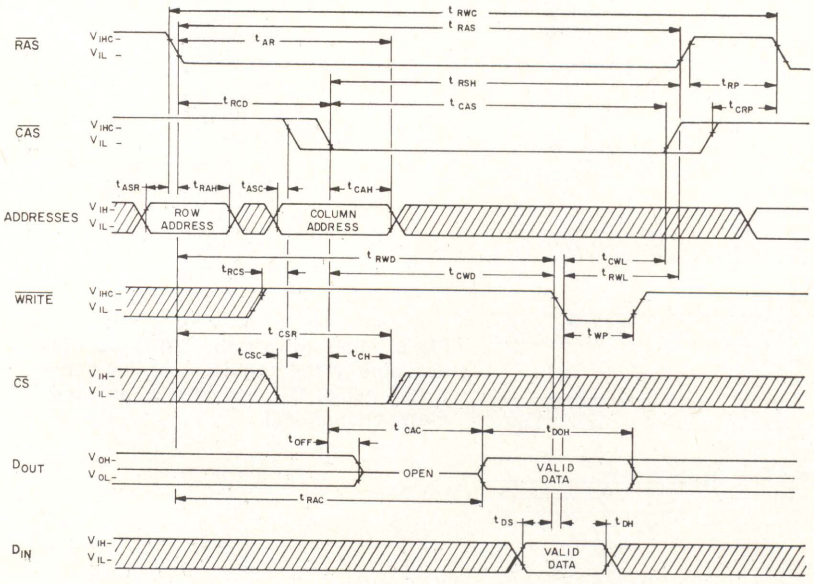


Fig 8 4027 read-write/read-modify-write cycle. This cycle starts as a read cycle, but as soon as characteristics allow, a write cycle is initiated. Write can be pipelined and started before D_{OUT} is stabilized. For read-modify-write, write D_{IN} is delayed until after D_{OUT}; thus, D_{IN} and WRITE are critical path signals and can influence this late "write cycle" time

TABLE 1

Write Signal Time Definitions For the 4096

Parameter	Definition
t_{WCH}	Overlap time between $\overline{WRITE}$ and $\overline{CAS}$ during an early write cycle. This is minimum time required to capture "write status" signal
t_{WP}	$\overline{WRITE}$-on pulse duration, any write cycle
t_{CWL}	Time from leading edge of $\overline{WRITE}$ to trailing edge of $\overline{CAS}$. This is effective write time on a late write cycle and time by which cycle must be extended to do a RW cycle
t_{DS}	Data setup time. Time from stable write data to beginning of $\overline{WRITE}$-on (in a late write) or to beginning of $\overline{CAS}$-on (in an early write). (Note: In an early write, where $\overline{WRITE}$ comes on before $\overline{CAS}$, leading edge of $\overline{CAS}$ triggers write operation. In a late write, leading edge of $\overline{WRITE}$ triggers write operation)
t_{DH}	Data hold time. Time follows initiation of a write operation ($\overline{WRITE}$-on or $\overline{CAS}$-on, whichever is later) during which write data must be held stable. This is time required to capture data in a latch
t_{MOD}	A system application-related parameter. Time required for D_{OUT} to be modified to form D_{IN} for a RMW cycle, external to memory array
t_{RWC}	Minimum RW cycle time, assuming some fixed transition time for signals, where they add to cycle time. This parameter is derived as sum of a number of other parameters: $t_{RWC} = t_{RCL}$ (max) $+ t_{CAC} + t_{CWL} + t_{CRL} + t_{RP} + 5t_T$

TABLE 2

Write Signal Time Definitions For the 4027

Parameter	Definition
t_{WCR}	Minimum time between beginning of cycle ($\overline{RAS}$-on) and trailing edge of $\overline{WRITE}$, during an early write only
t_{WP}	$\overline{WRITE}$-on pulse duration, any cycle (same as for 4096)
t_{RWL} and t_{CWL}	Minimum times between leading edge of $\overline{WRITE}$ and end of $\overline{RAS}$ and $\overline{CAS}$, respectively; parameters are numerically equal. They define effective time required to perform a write operation, and time by which a read cycle must be extended after valid write data to perform a RMW cycle
t_{DS}	Data setup time (see definition Table 1)
t_{DH}	Data hold time (see definition Table 1)
t_{DHR}	Minimum time during which write data must be held stable relative to $\overline{RAS}$-on, in early write cycle. This is an additional constraint on how long data must be held in an early write cycle. It applies and is the limiting parameter on data stable time when t_{RCD} is less than pseudomaximum value specified [t_{RCD} (max)]
t_{RWD} and t_{CWD}	Parameters describe earliest times that a write operation can start ($\overline{WRITE}$-on) without disrupting the valid D_{OUT} on a RW cycle. They define minimum delay from $\overline{RAS}$-on or $\overline{CAS}$-on to $\overline{WRITE}$-on. Value of t_{CWD} is typically 75 ns less than t_{CAC}. This implies that during a RW cycle, writing can start 75 ns before D_{OUT} is stable. This makes possible a RW cycle that is shorter than a RMW cycle. If $\overline{WRITE}$-on occurs before specified maximum values of t_{RWD} and t_{CWD}, valid read data will not be guaranteed
t_{RWC}	Minimum time needed for a RW cycle when full advantage is taken of read and write overlap capability of the 4027: $t_{RWC} = t_{RCD}$ (max) $+ t_{CWD} + t_{RWL} + t_{RP} + 3t_T$ This is different from 4096 t_{RWC} because of inability of 4096 to overlap read and write
t_{RMW}	System related cycle time is same as t_{RWC} of 4096 except that t_{RCD} (max) is substituted for t_{RCL} (max)

(max). For most parts this is at least 10 ns. A typical application is in a system with error correction.

The two RAM write cycles are defined as:

Write cycle—(Figs 5 and 6) Write data are available at the beginning of the cycle so that the write operation starts at the beginning. In this mode, D_{IN} and $\overline{WRITE}$ signal times are not in any critical path for determining cycle time; thus, they are completely non-critical. This cycle is often called an "early write."

Read-write cycle—(Figs 7 and 8) This cycle starts as a read cycle, but as soon as the device specification and characteristics allow, a write operation is started. In some devices (4096), write cannot start until after read D_{OUT} has stabilized; otherwise, the stabilization of D_{OUT} will be disrupted and errors can occur. In other devices (4027), the write operation can be pipelined and started before D_{OUT} is stabilized. In both of these situations, the $\overline{WRITE}$-on timing is in the critical path for cycle time. The RMW variant of this operation is one in which the write D_{IN} is delayed until after D_{OUT}. As a result, both D_{IN} and $\overline{WRITE}$ become critical path signals and can influence cycle time. This cycle is often called a "late write." Write parameters for the 4096 and 4027 are numerous, complex, and different. Write signal time definitions for the 4096 and 4027 are given in Tables 1 and 2, respectively.

Differences in Characteristics

Characteristics of the 4096 and 4027 RAMs differ in logic as well as in specific timing parameters. Logic differences show up as the presence or absence of some of the timing parameters. Tables 3 and 4 compare the timing parameters of the 4096 and the 4027. The 250-ns (t_{RAC}) 4096-6 and 4027-4 and the 200-ns (t_{RAC}) 4027-3 devices serve as the basis for this comparison.

RAMs listed in Table 3 do not differ greatly from each other in terms of access and cycle times. Within these times, however, the balance between individual parameters does vary. t_{RCD} (min) for the 4027 is one-half of the t_{RCL} of the 4096 for equal access times. This is compensated for by a longer t_{CAC} in the 4027. The longer multiplex window of the 4027 (50 ns versus 40

TABLE 3

Basic Read Cycle Parameters*

Parameter	4096-6	4027-4	4027-3
$t_{AH(R)}$	60	35	25
$t_{AS(C)}$	0	−10	−10
t_{RCL} (min) (t_{RCD})	70	35	25
t_{RCL} (max) (t_{RCD})	110	85	65
Δt_{RCL} (t_{RCD})	40	50	40
t_{CAC}	140	165	135
t_{RP}	115	120	120
t_{RC}	395	400	350
t_{RAC}(calculated)	260	260	210
t_{RAC}(spec)	250	250	200
t_{CRL}	50	—	—
t_{CRP}(min)	—	0	0

*All times are given in nanoseconds

TABLE 4

Basic Write and Read/Write Cycle Parameters*

Parameter	4096-3	4027-4	4027-3
t_{WCH}	110	75	55
t_{WCR}	—	160	120
t_{WP}	110	75	55
t_{RWL}	—	165	135
t_{CWL}	110	165	135
t_{DS}	0	0	0
t_{DH}	110	75	55
t_{DHR}	—	160	120
t_{CWD}	—	90	80
t_{RWD}	—	175	145
t_{RWC}	515	490	295
t_{RMW}	515	575	495

*All times are given in nanoseconds

TABLE 5

Timing Signal Definitions

Parameter	Definition
t_{CAH}	Y address hold time relative to $\overline{\text{CAS}}$-on
t_{CH}	CS (chip select) hold time relative to $\overline{\text{CAS}}$-on
t_{CHR}	CS hold time relative to $\overline{\text{RAS}}$-on
t_{AR}	Y address hold time relative to $\overline{\text{RAS}}$-on
t_{CSC}	Chip select (CS) setup time relative to $\overline{\text{CAS}}$-on
t_{DOH}	Data out hold time relative to time it becomes stable for a long period during which chip is idle
t_{OFF}	Time required for valid data out from previous cycle to go to float state after $\overline{\text{CAS}}$-on
t_{RAS}	Minimum duration of $\overline{\text{RAS}}$-on
t_{RC}	Minimum read cycle duration
t_{RCH}	Read command hold time relative to $\overline{\text{CAS}}$-off
t_{RCS}	Read command setup time relative to $\overline{\text{CAS}}$-on
t_T	General symbol used for transition time of a signal
t_{WCS}	Write command setup time relative to $\overline{\text{CAS}}$-on

ns) makes it easier for the system to achieve the fastest possible access time.

These differences have their primary impact when a 4027 is used in an application or specification based on 4096 timing. The 4027 has a longer access time of 50 ns; to compensate, a 200-ns 4027-3 would be required to replace a 250-ns 4096-6.

Logic differences show up in parameters t_{CRL} and t_{CRP}. Since the 4027 has a greater timing flexibility, it is logically compatible with a system timed for a 4096.

Write and read-write cycle parameters for the same three RAMs are compared in Table 4. For a given access time, minimum RW cycle time for a 4027 is less than that for a 4096. However, in a RMW mode, the 4027 has a longer cycle time. To achieve an equivalent t_{RMW}, a part with a shorter t_{RAC} must be used.

Careful examination of the published data sheets will reveal other timing parameters (see Table 5). These parameters are either non-critical or self-explanatory so that additional discussion is not needed. This does not mean, however, that they can be ignored or violated. All parameters included in the data sheets serve a definite purpose and must be evaluated in any design.

Conclusion

Although similar, the 4096 and 4027 16-pin 4k RAMs have important dynamic differences. Similarities include 16 pins, address multiplexed, identical pinouts, and the same supply voltages and interface signal levels. Differences exist in logic as well as in timing. The 4027 can be used in a system timed for the 4096, but there is degradation in performance. At least 50 ns are lost in access time and over 100 ns are lost in a RMW cycle. In addition, there are differences in many secondary characteristics. The most serious of these relates to the maximum operating voltages to which the parts can be subjected. The 4096 can safely take V_{DD} values of 20 V or more; however, this voltage would result in destruction of the 4027, which has a maximum safe limit of closer to 16 or 17 V.

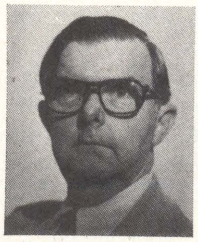
The designer must know the parts thoroughly and understand their similarities and differences. Otherwise, serious operational difficulties will be encountered.

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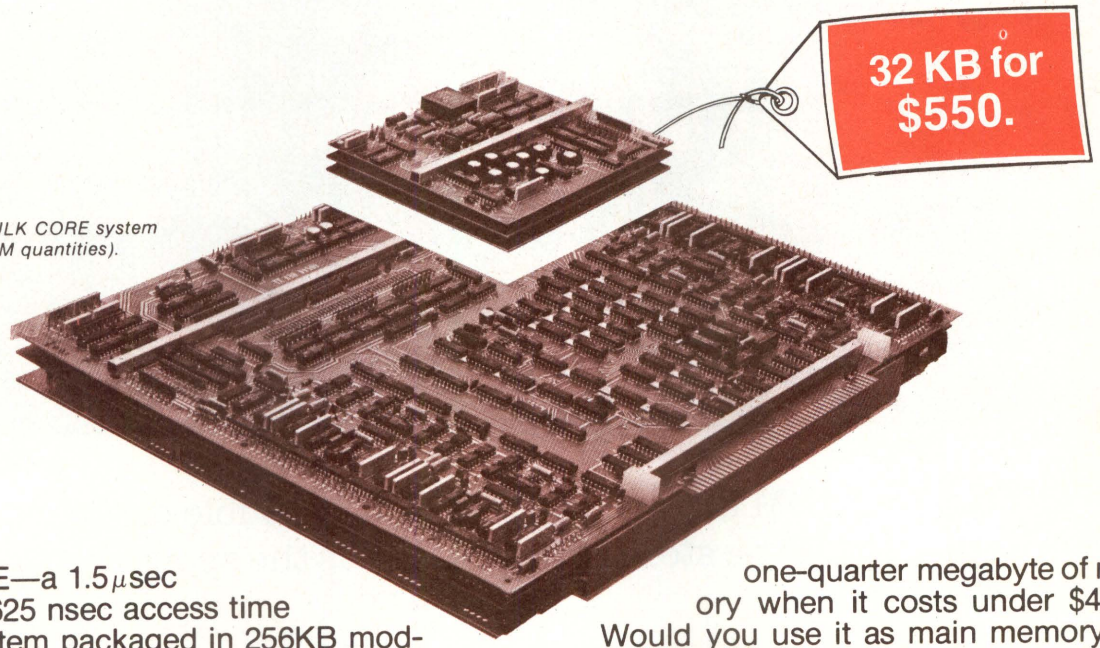


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By treating microprograms as task partitions of a single program in a time-slicing technique, the function modularity provided by multiprocessors is obtained along with the system design simplicity of a single microprocessor

Time-Slicing Offers an Alternative To Multiprocessor Systems

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Ever-decreasing costs of microprocessors, coupled with increasing complexity of microprocessor-based systems, have sparked a great deal of interest in multiprocessor systems. In these systems, each microprocessor is assigned a specific task which it performs under control of either individual or shared programs and data in memory. Among the advantages of multiprocessor systems are modularity of function and increased processing efficiency; however, these advantages are not obtained without penalty. The multiprocessor approach usually requires complex programming schemes to link individual programs together and establish system protocols; and, typically, external hardware is needed to perform sequencing and bus allocation functions. Degree of complexity and amount of overhead hardware are, of course, dependent upon the application and the microprocessor—but it is apparent that the multiprocessor approach is not necessarily the panacea that it at first appears.

What, then, are the options? The arrival of a new breed of microprocessors with features specifically designed to enhance multiprocessor operations will no doubt eliminate some of the existing drawbacks, but their appearance is in the distant future. New system concepts may also evolve to ease the overhead penalties and simplify intercommunication and control of multiprocessors. However, there is another option—multitasking under the control of a single microprocessor. Although this may seem like a step backward, there are methods of obtaining the modularity advantages provided by multiprocessors while maintaining the system design simplicity provided by a single-microprocessor system. One

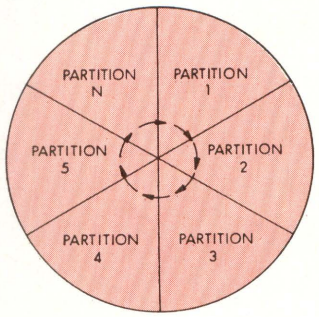


Fig 1 Time-slicing technique for allotting processing time among partition programs. After each T/N time interval, system control is transferred to the next active partition. A time slice of 150 ms allows execution of 10,000 instructions, for an average instruction time of 15 μs

such method is "time-slicing" or assigning definitive time intervals for processing task partitions, or portions, of the overall system program. This method may prove advantageous in a variety of applications until the "new breed" of microprocessors arrives.

A small-scale data processing system is described in this article to illustrate application of the time-slicing technique for multitask systems. The single-chip 16-bit PACE (processing and control element) microprocessor (manufactured by National Semiconductor Corp) was selected as the example central processing unit (CPU) because of its prioritized multilevel interrupt structure and its halt/continue feature that allow easy implementation of direct memory access (DMA) schemes.

Time-Slicing for Multitasking

The time-slicing technique allows multiprograms to be treated merely as partitions of a single microprocessor program (see Fig 1). Specific system tasks are allotted to individual time-slices and are serviced on a "round-robin" basis. The number of individual programs (which form a multiprogram system) and the duration of each time-slice depend on system tasks to be performed and microprocessor capabilities. For example, if a microprocessor has an average instruction execution time of 15 μs, a time-slice of 150 ms will allow execution of approximately 10,000 instructions. If six individual programs are to be serviced, a complete cycle is made in

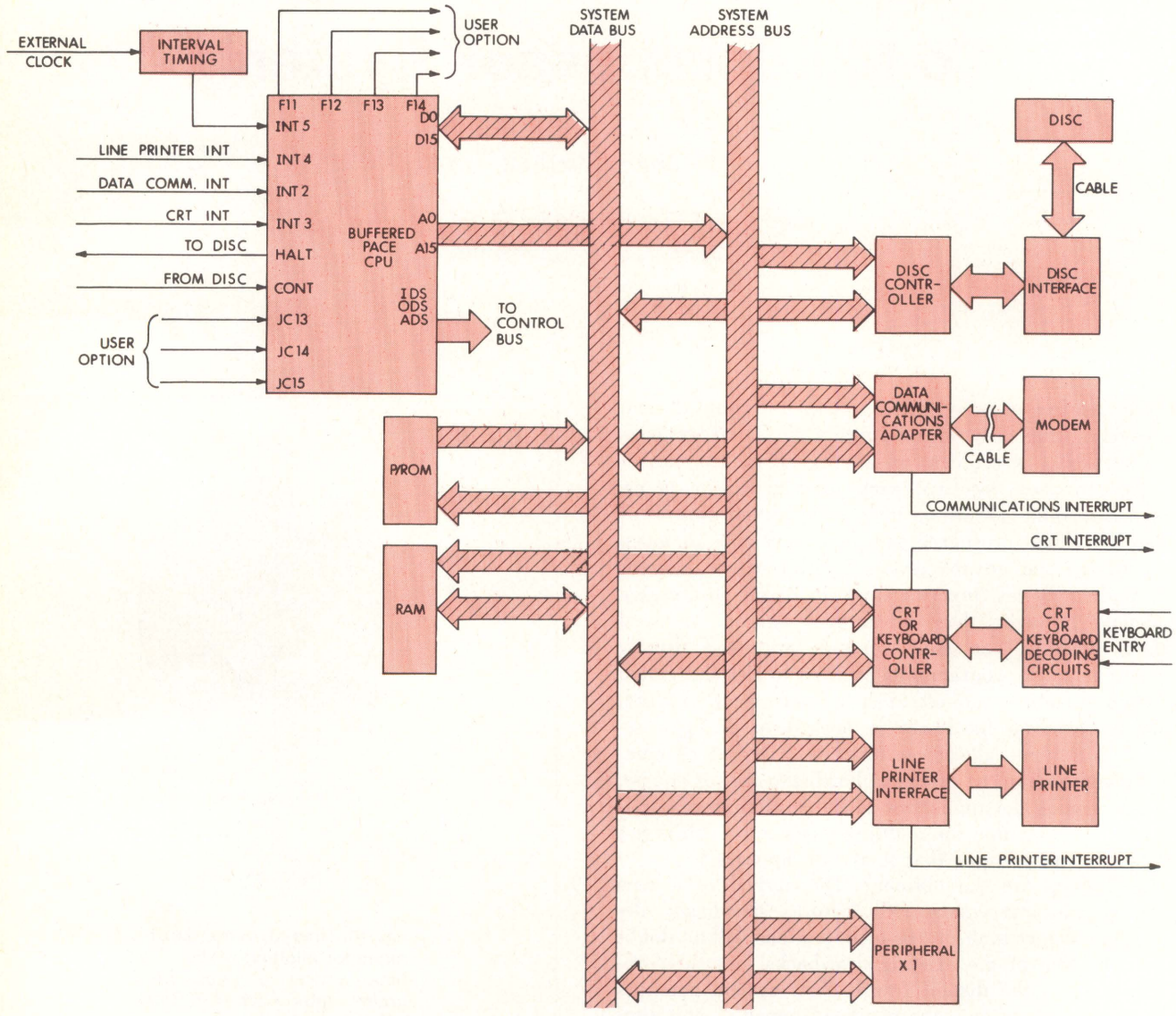


Fig 2 A small scale microprocessor system suitable for business data processing. Using buffered PACE as a CPU, this system functions effectively as an online interactive data processor or as a retail data transaction processor. All peripherals can communicate with the CPU simultaneously. A fast transfer of controls to the disc controller permits DMA operation. Other peripherals transfer information on an I/O basis. All peripherals are connected to the system data bus and are accessed through the system address bus

less than 1 s (including software overhead). In this scheme, the microprocessor executes each program for 150 ms and then switches over to the next program in sequence. If the microprocessor has an interrupt capability, variable time-slices can be established by the programmer using an external counter driven by an external clock.

Microprocessor CPU

A block diagram of a small-scale data processing system using the chosen microprocessor as a CPU is shown in Fig 2. This system can be configured to function as an online interactive data processing system or for retail transaction processing. Disc controller, data communications adapter, cathode-ray tube (CRT) display, line printer, and other peripherals are connected to the system data bus and accessed through the address bus. The microprocessor treats peripherals as memory locations; therefore, all memory reference instructions can be used with peripherals. More peripherals can be added by assigning different addresses.

Under this approach, the disc is the only device capable of transferring blocks of data using DMA control. All other connected peripherals transfer data on a program-controlled input/output (I/O) basis. The CRT is used as an interactive terminal with the data communications adapter and the line printer as supporting peripherals. Partition programs for these devices have interrupt service routines associated with them to transfer data. The disc controller program uses the HALT (which is also priority interrupt, level 0) and CONTINUE signals to transfer data in a DMA mode. The interval timer that is used to control the partition processing time is tied to the lowest priority interrupt, level 5. Other priority interrupt assignments are: level 2, data communications; level 3, CRT; and level 4, line printer. Level 1 is not available in this system.

System Operation

Fig 3 shows the system state diagram and Fig 4 depicts the overall system flowchart. The power-on routine of the program clears all software pointers and flags. The system then enters the system initialize routine and waits for the operator to start the system. Control parameters are entered via the CRT terminal. For the simple case considered, the system provides two alternatives. (1) New partition programs can be entered using a peripheral which is initialized by the operator; this mode also stores the required pointers in preassigned locations. (2) For preassigned locations, the partition program counter pointer can be entered for the desired partition program if partition programs are already stored. In addi-

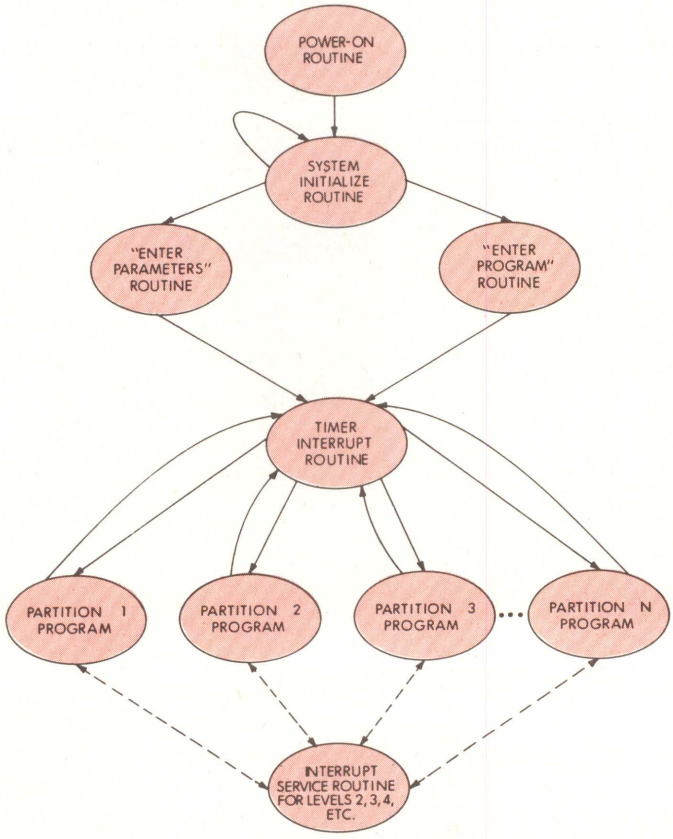
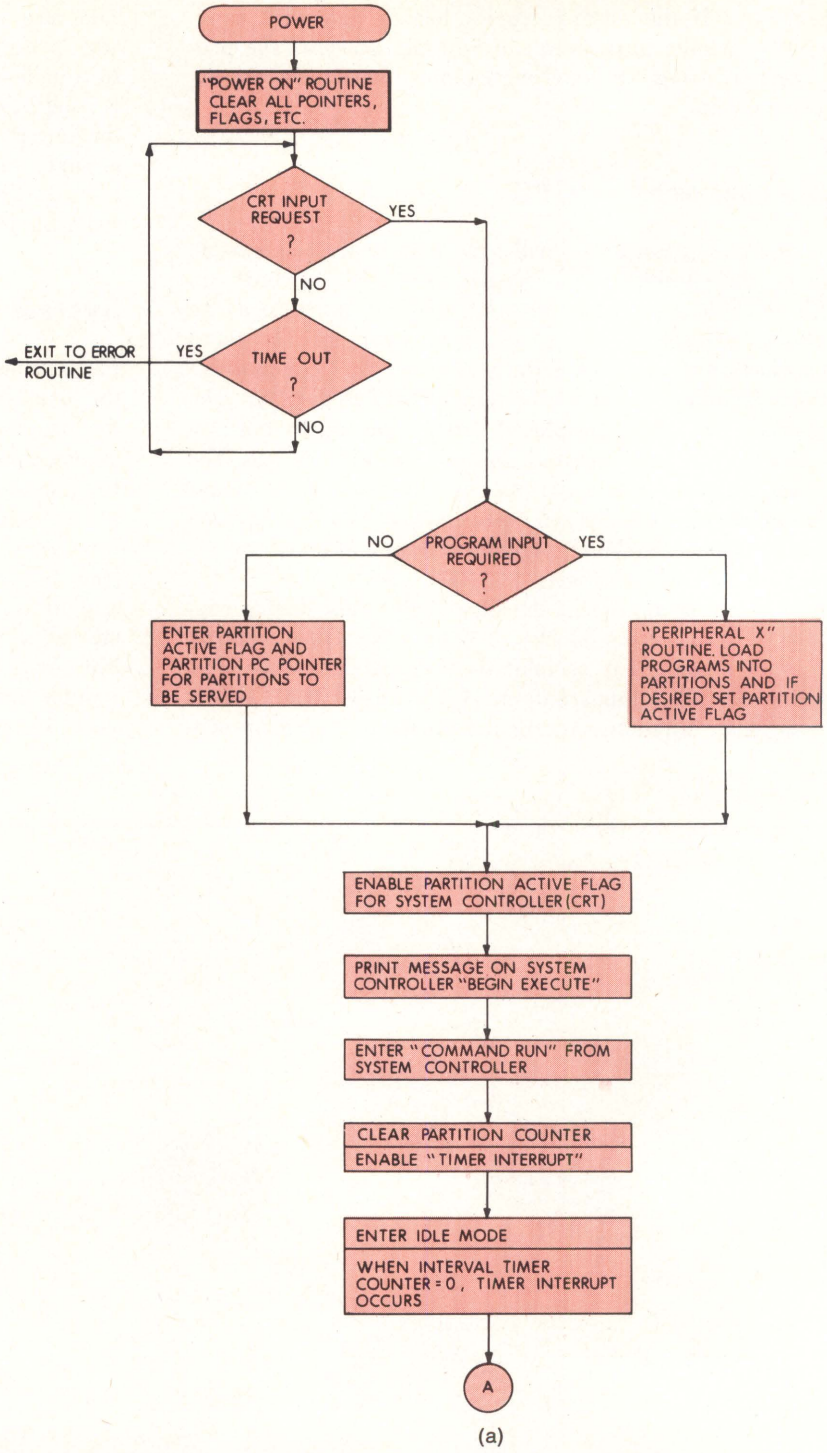


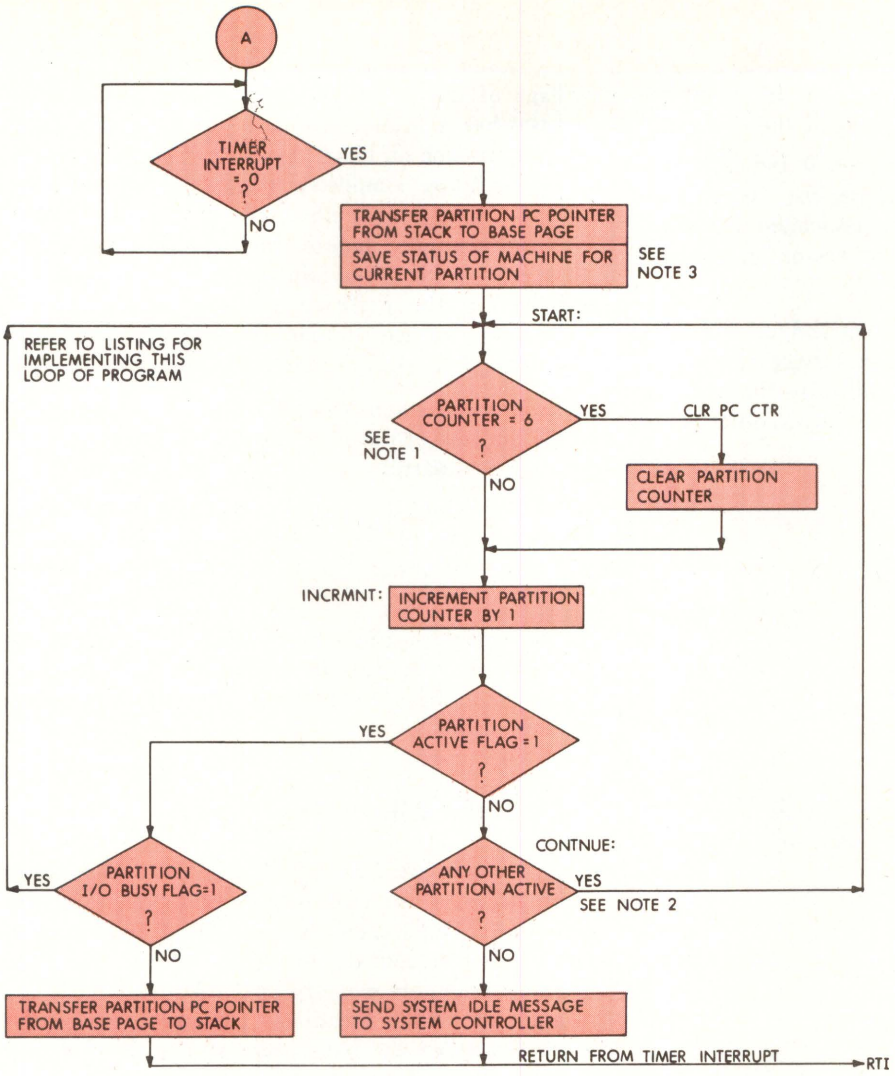
Fig 3 System state diagram. Power-on routine clears all pointers and flags. Then, system enters system initialize routine and awaits operator inputs. If new partition programs are desired, they are loaded using a peripheral in the enter program routine. If partition programs are already stored, enter parameters routine initializes system by entering partition program counter pointer and partition active flag. Based on interval timer count and flag status, timer interrupt routine transfers control among the partition programs. The current partition program can be interrupted by any interrupting condition in the system



(a)

tion, all partitions that need to be served should be activated by setting the associated partition-active flag. Any additional parameters that the programmer desires should be entered from the CRT. At this point, the system is completely initialized and enters run mode.

Control of the system is transferred to the first partition program. This program loads the external interval timer (a counter) with the precalculated interval count; then, the interval timer proceeds to count down to zero. Zero count is reached in a time interval depending on the period of the external clock used. For example, an external clock frequency of 1 kHz gives a period of 1 ms for each interval count. When the interval timer counts to zero, it interrupts the microprocessor. Then, the timer



NOTES:

1 MAXIMUM PARTITION COUNT = THE NUMBER OF PARTITIONS IN SYSTEM. IN THIS CASE, IT IS EQUAL TO 6

2 THE "SYSTEM CONTROLLER" PARTITION IS ALWAYS ACTIVE AND IS NOT TESTED FOR IDLE CONDITION.

3 DO NOT USE ON-CHIP STACK FOR SAVING STATUS, TO AVOID COMPLICATIONS IN UPDATING STACK POINTER

(b)

Fig 4 System flow chart. Power-on and system initialization routines (a), along with operator data entry, set up new or already stored partition programs and system flags. Then, run mode clears partition counter and enables timer interrupt routine (b). When timer counts to zero, it interrupts CPU and enables timer interrupt service routine. This routine checks current partition program, and flag status for next partition program. In this system, when partition counter reaches 6, control is transferred back to partition 1 program, and system operation continues in this "round-robin" processing technique

interrupt service routine transfers system control to the next partition program. This is achieved simply by loading the current partition program counter pointer of the next partition into the processor's program counter.

The timer interrupt service routine keeps track of the partition being served using a software partition counter. In this case, when the partition counter reaches 6, it is cleared and system control is transferred to partition program 1. The timer interrupt service routine, before transferring control to the next partition, examines the status of two flags associated with the next partition.

Partition Active Flag—When set, flag indicates that the partition requires processing time to execute its program.

The flag is set by the system operator or, in an interactive program, by some other program of the system.

I/O Busy Flag—When this flag is set, it indicates that, after partition program execution begins, the program has entered interrupt mode and the associated device will transfer information to the microprocessor on an interrupt basis.

If the partition active flag is not set and/or if the I/O busy flag is set, the timer interrupt service routine advances the partition counter by 1 and skips the next partition. These flags can be combined with other status flags of the partition to form a partition status word. PACE has a branch-on-condition instruction that can directly branch on bits 0, 1, and 2 of accumulator 0 (AC0). For software simplicity, these flags should be assigned bit positions 0, 1, 2, etc.

As mentioned before, each partition program has associated with it certain parameters that are required either by the partition program or by the associated interrupt service routine. These are the program counter pointer, "A" pointer, and "B" pointer.

Program Counter Pointer—16-bit pointer which stores the address of the next instruction to be executed in the associated partition.

"A" Pointer—16-bit word typically used to designate the number of characters to be transferred in case of I/O operations and to be processed in arithmetic operations. It is user selectable for other uses as well.

"B" Pointer—16-bit word typically used to designate the starting address in memory to load or unload data characters in I/O operations. It is also user selectable for other uses.

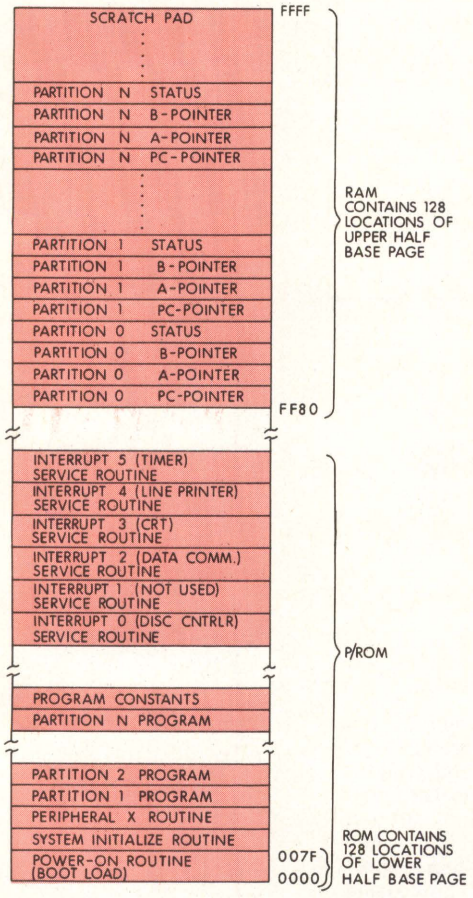


Fig 5 Memory map. Total memory contains 65,536 locations in RAM and p/ROM. Parameters are stored in part of memory, called base page, which has 256 locations. For programmer convenience, base page can be split into upper and lower halves, each made up of 128 locations. Upper half is stored in RAM, FF80 to FFFF, while lower half is included in p/ROM, 0000 to 007F. These locations can be directly accessed from any part of the memory

Memory Allocation

Parameters are stored in a section of memory that can be accessed directly from any location in the entire memory; total memory consists of read-write random-access semiconductor memory (RAM) and programmable read-only memory (p/ROM) and contains a maximum of 65,536 locations. The parameter memory section is called the base page, and is 256 locations long. PACE allows the programmer to split the base page into two sections. Using this split-base-page mode, the bootload program that initializes the system can be stored in p/ROM using the lower half of the base page, and all partition status and pointer parameters can be stored in RAM using the upper half of the base page. The upper half base page ranges from hexadecimal locations FF80 to FFFF, the lower half base page from 0000 to 007F (see Fig 5).

Data Communications Controller

An example of a partition program to control the data communications adapter is given in Fig 6(a) along with the flowchart for the associated interrupt service routine [Fig 6(b)]. The partition program is written for a general-purpose communication scheme. This type of adapter can be connected to a half-duplex switched line or private line. It can perform a dial-out function and can respond to a ring from a switched line.

The initialize routine shown in the program flowcharts gives parameters like request to send, data terminal ready, word length of characters, even/odd parity, type of block-check character, etc. Refer to the specifications of the Electronic Industries Association's RS-232-C standard for descriptions of these parameters. Additional

Sample System Program Listing

```
START:      LI      AC0, 6              ; Set ACU0 = 6
            SKNE    AC0, PCTR           ; Check if partition counter = 6
            JMP     CLRPCTR             ; Jump to clear partition counter
INCRMNT:    ISZ     PCTR                ; Increment partition counter by '1'
            LI      AC0, MASK 1         ; Set AC0 = MASK 1 value
            AND     AC0, PSTATUS        ; to check if partition is active
            BOC     PSIGN, CONTINUE     ; Branch to continue if AC0 > 0
            LI      AC0, MASK 2         ; Set AC0 = MASK 2 value
            AND     AC0, PSTATUS        ; to check if partition I/O busy flag is set
            BOC     PSIGN, START        ; Branch to START, if AC0 > 0
            LD      AC0, PCPTR          ; Load partition PTR → AC0
            PUSH    AC0                 ; Transfer AC0 → STACK
            RTI                         ; Return from interrupt
CONTINUE:   LD      AC0, SYSTEM         ; Transfer system active → AC0
                    ACTIVE
            BOC     PSIGN, START        ; If any partition is active, loop back
                                        ; to start (AC0 > 0)
            LI      AC0, SIDLE          ; Set AC0 = System IDLE code,
            ST      AC0, SCTRL          ; Transfer AC0 → System controller mail box
            RTI                         ; Return from interrupt
CLR PCTR:   LI      AC0, 0              ; Set AC0 = 0
            ST      AC0, PCTR           ; Set PCTR location = 0
            JMP     INCRMNT             ; Jump to increment
```

Definitions

MASK 1 = Mask value to mask off required bit of partition status word to check if partition is active
MASK 2 = Mask value to mask off the required bits of a partition status word to check if partition I/O busy flag is set
PCTR = Partition counter
PCPTR = Partition program counter pointer
PSTATUS = Partition status word. This word contains partition active and I/O busy flag status information

parameters are required when the asynchronous or synchronous mode of transmission is established.

In receive, transmit, dial, and detect-ring modes shown in Fig 6, the I/O busy flag is set after initialization because the data communications adapter is virtually waiting for some response from the modem end. The flowchart [Fig 6(b)] shows when the I/O busy flag is cleared for each mode. The specific response can take a varying amount of time (eg, the ring may not occur at all).

In some cases, like waiting for a clear-to-send response from the modem, a time-out loop should be added in series with I/O busy to eliminate the possibility of waiting indefinitely and holding up the partition. The timer interrupt service routine, when it addresses the data communications partition, detects the partition I/O busy flag set, skips servicing that partition, and moves the system to the next partition. This eliminates wasting CPU processing time while waiting for responses which are asynchronous in nature.

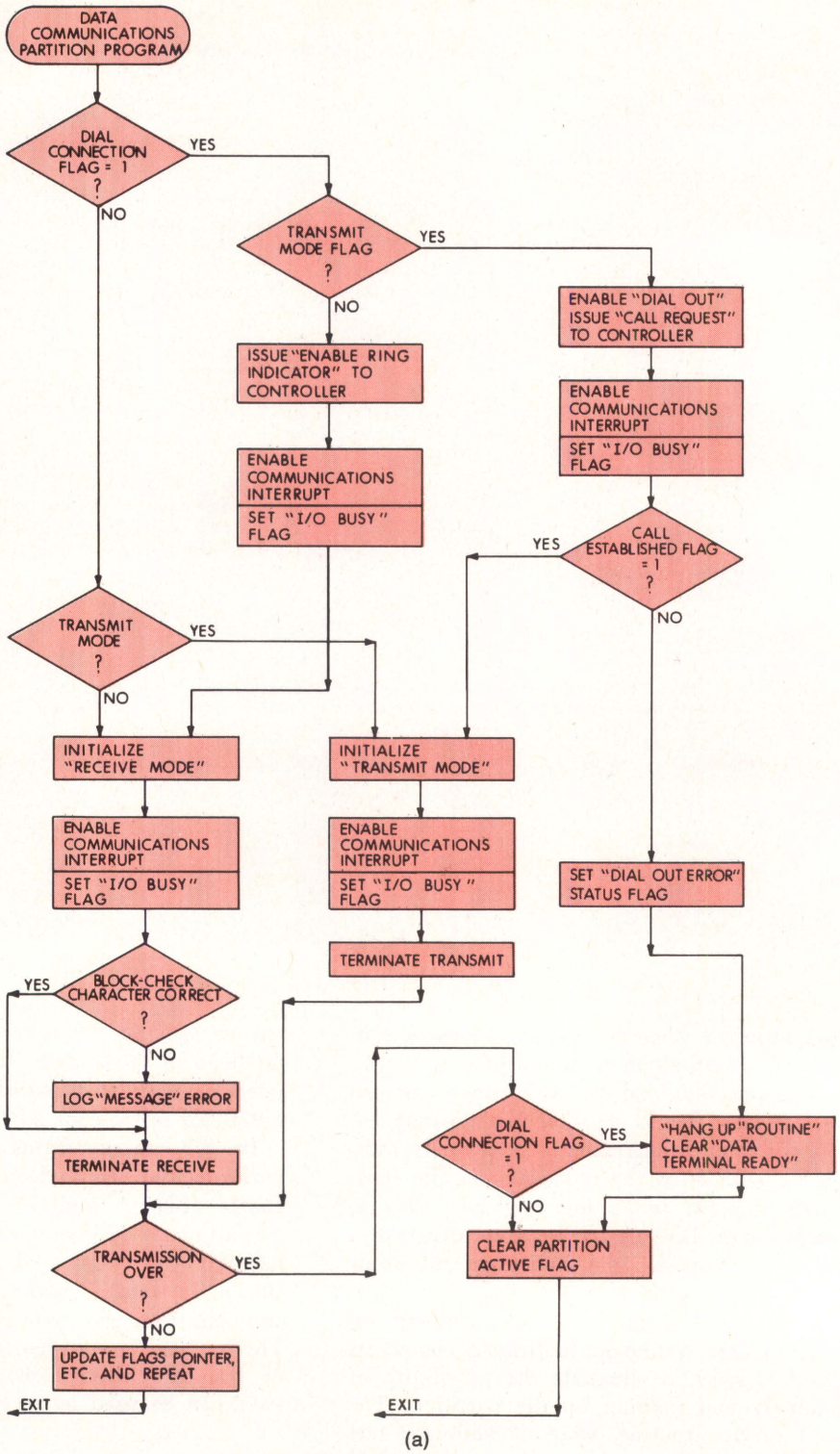
The interrupt service routine shown for the data communications adapter first reads in the interrupt status word generated by the adapter. Each bit of the status word has a significant meaning as shown in Fig 7. The program knows what it is looking for either by setting flags in the microprocessor or by setting some flip-flops in the adapter hardware; eg, the adapter will interrupt with ring indicator (RI) status only if it is initialized to look for RI by the "enable RI" instruction.

In each interrupt status condition, the interrupt routine performs the required function as shown in the flowcharts (Figs 6 and 7). Familiarity with the binary synchronous (BiSync) communication procedure is necessary to fully understand the implied functions shown. In transmit and receive modes, detection of control characters sets certain flags to establish these modes. The last flag is set when the end of text (ETX) or end of transmit (EOT) character is detected. Note that PACE can be used in an 8-bits/word mode.

DMA Transfer

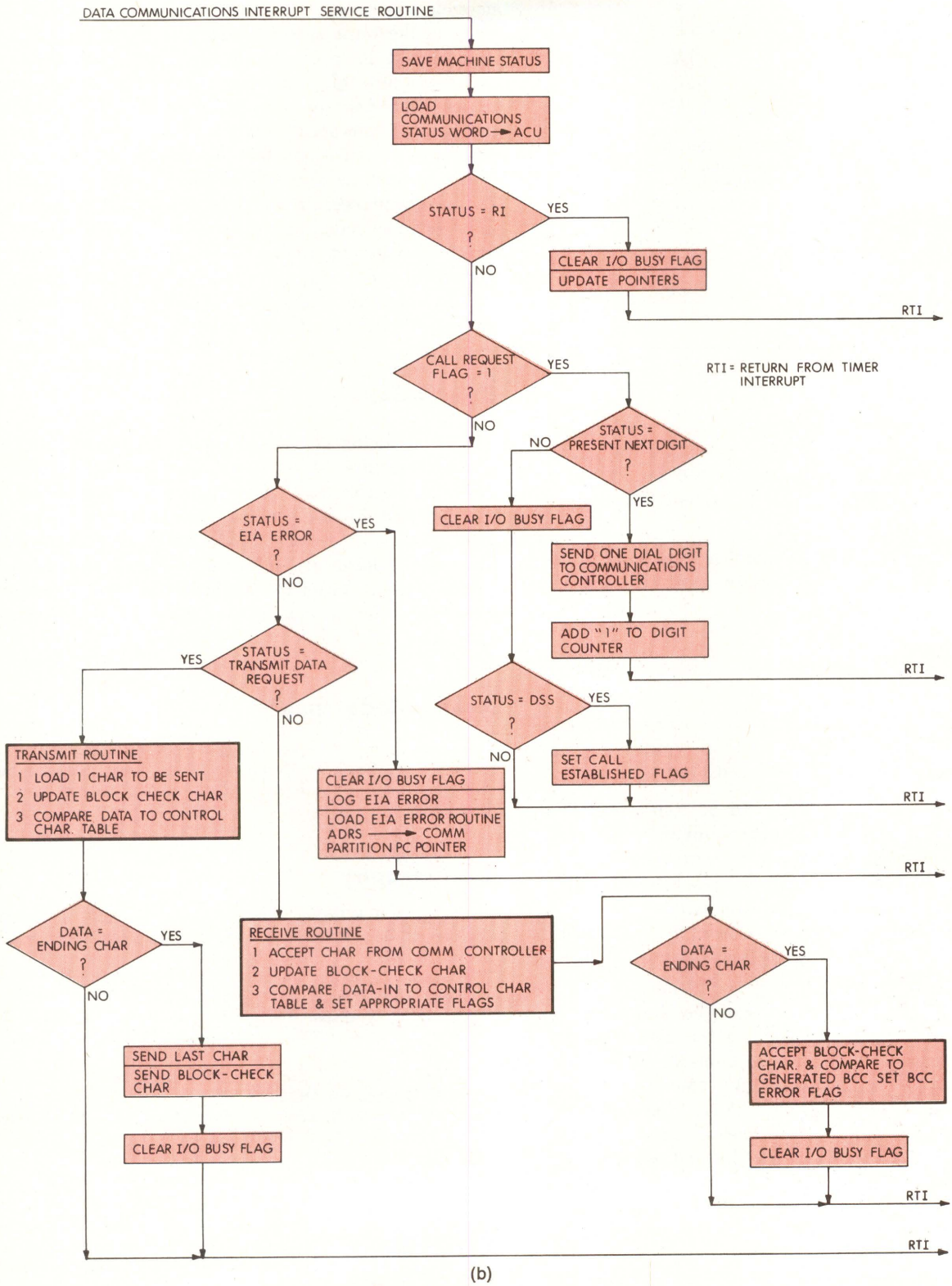
DMA transfer for the disc controller is initiated in the following manner:

(1) The partition program initializes the disc controller by issuing the track address, sector address, starting address of data in memory, number of characters to be transferred, read/write operation, etc.



(a)

Fig 6 Data communications partition program and interrupt service routine flow charts. Partition program (a) illustrates a general-purpose data communications system for a half-duplex switched or private line. After a transmit, receive, dial, or ring mode is initialized, the associated I/O busy flag is set, and the system waits for a modem response by enabling interrupts. This method will eliminate waste processing time because the communication partition will not be served until the modem response occurs, which will, in turn, reset the I/O busy flag. If response time is long-term, interrupt service routine (b) activates and transfers system to the next partition program while saving the status of the interrupted partition program


DATA COMMUNICATIONS INTERRUPT SERVICE ROUTINE
SAVE MACHINE STATUS
LOAD COMMUNICATIONS STATUS WORD → ACU
STATUS = RI ?
YES
NO
CLEAR I/O BUSY FLAG
UPDATE POINTERS
RTI
CALL REQUEST FLAG = 1 ?
YES
NO
RTI = RETURN FROM TIMER INTERRUPT
STATUS = PRESENT NEXT DIGIT ?
NO
YES
STATUS = EIA ERROR ?
YES
NO
CLEAR I/O BUSY FLAG
SEND ONE DIAL DIGIT TO COMMUNICATIONS CONTROLLER
ADD "1" TO DIGIT COUNTER
RTI
STATUS = TRANSMIT DATA REQUEST ?
YES
NO
STATUS = DSS ?
YES
NO
SET CALL ESTABLISHED FLAG
RTI
TRANSMIT ROUTINE
1 LOAD 1 CHAR TO BE SENT
2 UPDATE BLOCK CHECK CHAR
3 COMPARE DATA TO CONTROL CHAR. TABLE
CLEAR I/O BUSY FLAG
LOG EIA ERROR
LOAD EIA ERROR ROUTINE ADRS → COMM PARTITION PC POINTER
RTI
DATA = ENDING CHAR ?
YES
NO
RECEIVE ROUTINE
1 ACCEPT CHAR FROM COMM CONTROLLER
2 UPDATE BLOCK-CHECK CHAR
3 COMPARE DATA-IN TO CONTROL CHAR TABLE & SET APPROPRIATE FLAGS
DATA = ENDING CHAR ?
YES
NO
SEND LAST CHAR
SEND BLOCK-CHECK CHAR
CLEAR I/O BUSY FLAG
ACCEPT BLOCK-CHECK CHAR. & COMPARE TO GENERATED BCC SET BCC ERROR FLAG
CLEAR I/O BUSY FLAG
RTI
RTI

(b)

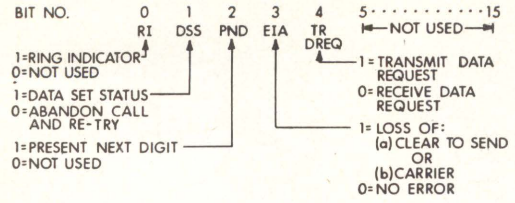


Fig 7 Interrupt status word generated by data communications adapter. Depending on status of bits 0 through 4, data communications interrupt service routine [Fig 6(b)] performs the required function. Bits 5 through 15 are not used

(2) The partition program then executes a HALT instruction which pulses the N-HALT output of PACE. At this point, bus control can be transferred for the disc controller, and the direct memory access transfer is started.

(3) When DMA transfer is complete, bus control is transferred back to PACE by raising the CONTINUE line in the required timing sequence.

Functional Capabilities

Using "A" pointer, "B" pointer, I/O busy flag, and partition active flag instructions, the following types of system functions can be implemented.

Data Transfer—A block of data can be transferred between a peripheral and the microprocessor under control of the partition program on an interrupt basis. The interrupt service routine transfers one byte of data, stores it at the address pointed to by pointer B, increments pointer B by 1, decrements pointer A (number of characters) by 1, and checks to see if pointer A = 0. If pointer A = 0, it clears I/O busy flag.

Control—The control functions can be implemented using a technique similar to the one for data transfer. For example, consider the process control system that consists of a digital-to-analog (D-A) converter and a multiplexed input analog-to-digital (A-D) converter. For such a system, the partition program can issue a digital value to the D-A converter which the end system uses to drive a device. After some delay, or when an asynchronous event occurs, a response in the form of an analog signal (feedback) needs to be examined. The program could be written such that the partition will enter a busy state while waiting for an analog response. In this case, the completion of a delay or asynchronous event can be tied to the interrupt input, and the interrupt service routine could be written to select an analog signal, convert it to a digital value, compare it to the expected digital value, and make certain decisions.

This example illustrates how devices other than peripherals can be interfaced and controlled by synchronizing external events into the system timing. Programs can also be written such that an event in one partition will start a chain reaction in other partitions, and direct them at a different program to control the system. It is possible to combine the data transfer and control functions in the same system using this technique.

It should be pointed out that combining the interrupt structure of a microprocessor to the partitions varies depending on the final application system and the type of microprocessor. A system could have combinations of partitions that do or do not require any interrupt input associated with them. Some partitions are exclusively processing the data collected by other partitions or independent of other partitions, and do not require an interrupt input associated with them.

PACE is used only as an example. Depending on the speed, complexity, and cost objective of the final system, other microprocessors could be used.

Conclusion

The time-slicing technique, combined with the interrupt structure of the PACE microprocessor, offers a powerful, flexible, and efficient system configuration that can be used in applications such as security systems, data processing systems, and process control systems. The modest hardware/software overhead and relatively simple system protocols required by the time-slicing technique offer a viable alternative to multiprocessor systems.

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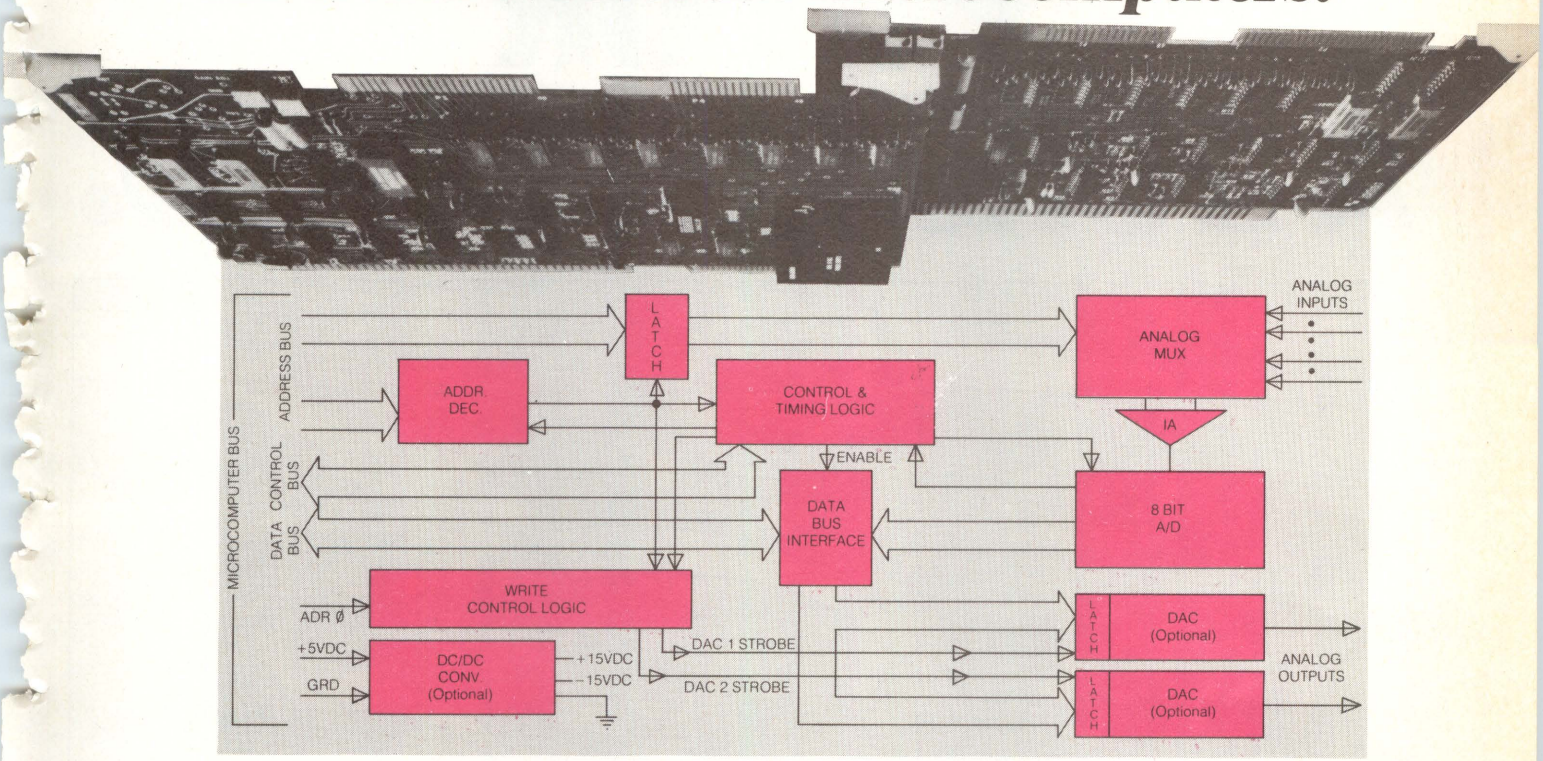
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Janak Pathak holds the MS degree in electrical engineering from Florida Institute of Technology and is currently pursuing the MBA degree at the University of Santa Clara. A microprocessor applications engineer at National Semiconductor, he has extensive experience in multiprocessor systems, data communications, and data acquisition systems.

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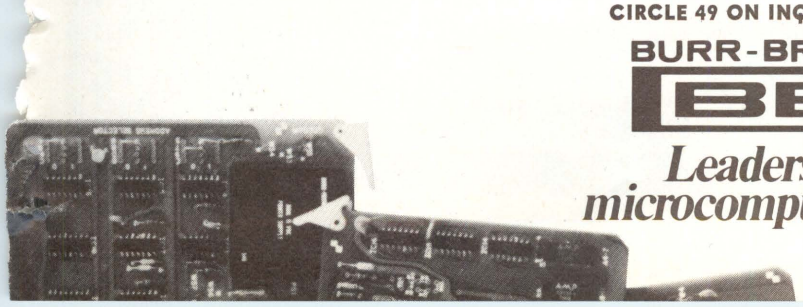
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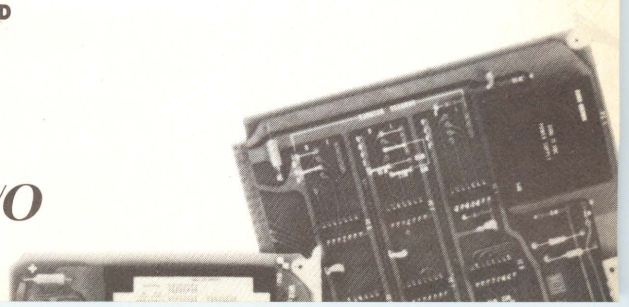
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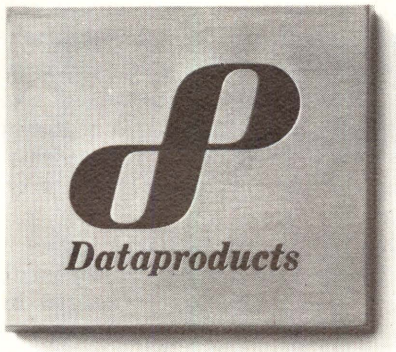
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A Microprocessor Controller for an Epitaxial Reactor

David Herberg, Nirmal Ratnakumar, and Peter E. Lobban

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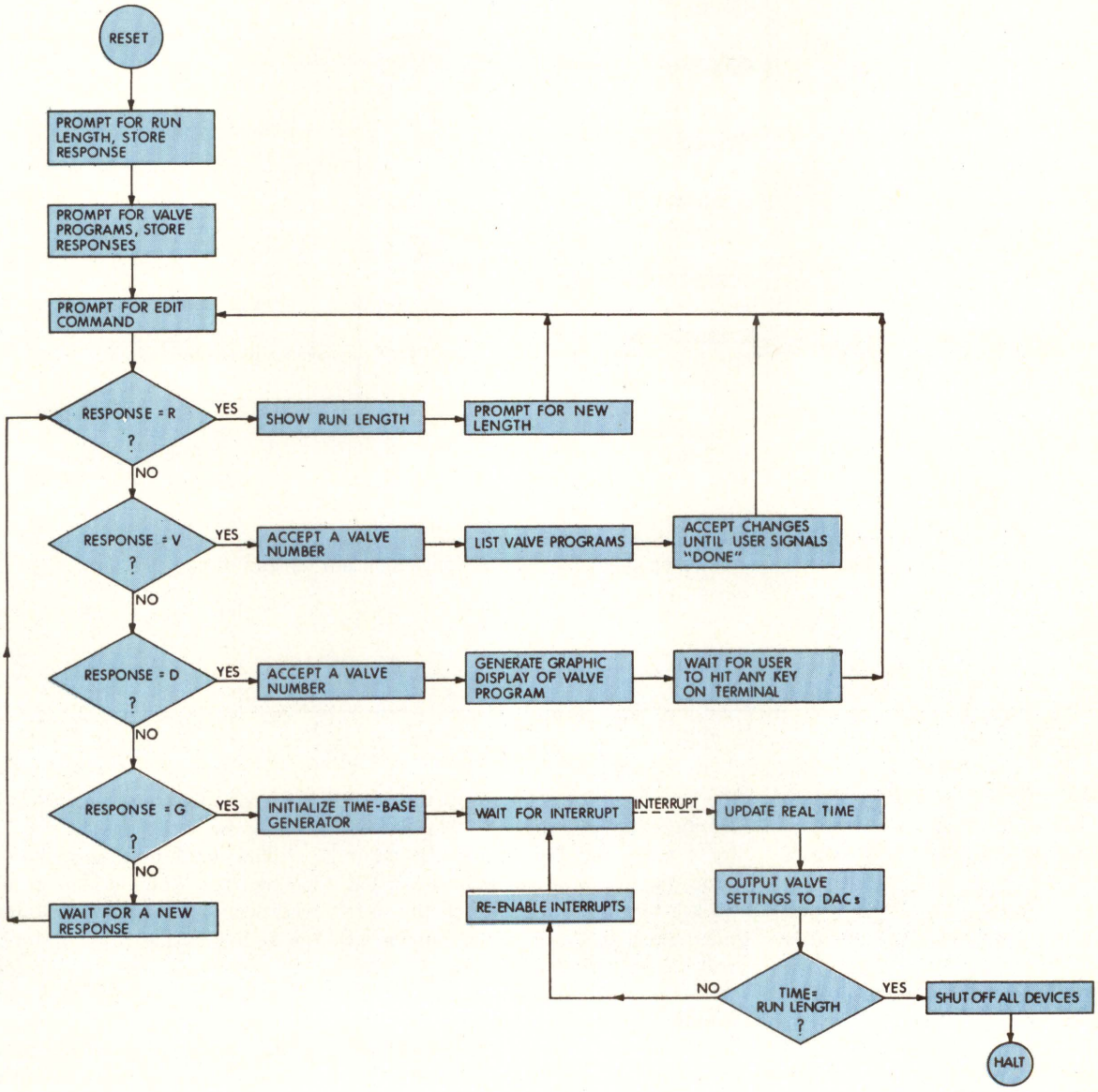
Regulation of gas flow rates in an epi-reactor by a microprocessor-based device serves to improve control of parameters during growth of epitaxial layers for production of ICs

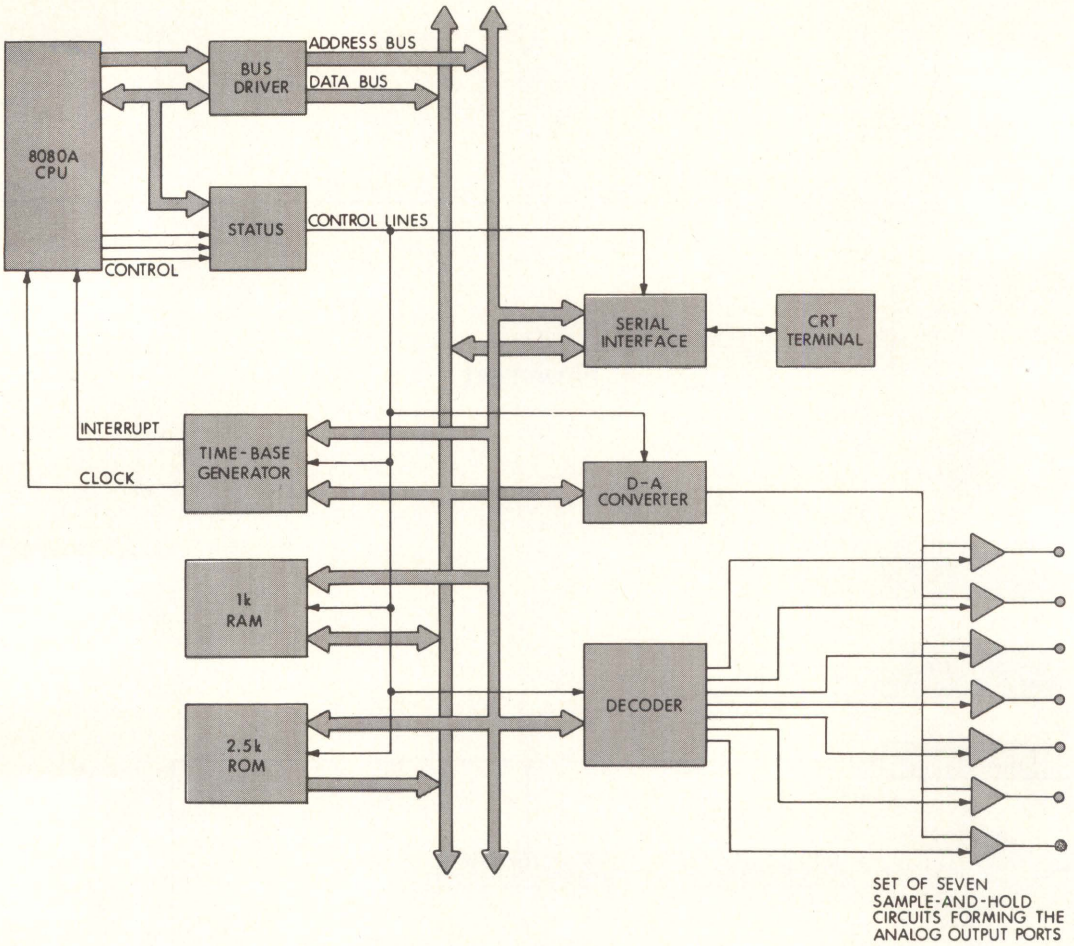
Epitaxial growth of silicon is one of the processing steps in the fabrication of integrated circuits. In a reactor used for that purpose, gases such as hydrogen, silane, and the dopants have to flow at different rates during different stages, and the flow rates must be adjusted for each run to realize the specific impurity profile and epi-layer thickness desired. A more accurate, repeatable, and convenient control over the process results when it is automated through a programmable microprocessor controller.

Regulation of gas flow is achieved by fitting each gas line with a mass-flow controller, which is a servo-operated proportional valve. Through associated electronics and feedback control, it converts a command voltage (0 to 5 V) to a proportional gas flow. A set of seven analog output ports from the microprocessor are connected to the command ports of the corresponding mass-flow controllers. During a run, the processor outputs to each port a voltage varying in time according to a user-specified "valve program," thus realizing the desired gas flow.

Before a run begins, the run length and valve programs are entered by the user via a CRT console. In this instance, it is a Lear-Siegler ADM-3 terminal interfaced to an Intel 8080A microprocessor by a Processor Technology 3P+S board. Memory includes 2.5k of 1702A UV-erasable p/ROM, and 1k of 2102 RAM. The valve programs are accepted in the form of valve setting-elapsed time pairs that realize a stepwise approximation to the desired gas flows; the software coordinates the input process by presenting various prompts to the user, such as "VALVE SETTING =" and "UNTIL TIME =". Each valve setting is a number ranging from 0.000 to 1.000, and each elapsed time is in the form XX:YY, where XX is the minutes portion and YY the seconds portion. The two numbers together constitute an "entry" in the valve program, and they occupy three consecutive bytes in the processor's RAM (the 8-bit quantiza-

Flowchart


RESET
PROMPT FOR RUN LENGTH, STORE RESPONSE
PROMPT FOR VALVE PROGRAMS, STORE RESPONSES
PROMPT FOR EDIT COMMAND
RESPONSE = R ?
YES
SHOW RUN LENGTH
PROMPT FOR NEW LENGTH
NO
RESPONSE = V ?
YES
ACCEPT A VALVE NUMBER
LIST VALVE PROGRAMS
ACCEPT CHANGES UNTIL USER SIGNALS "DONE"
NO
RESPONSE = D ?
YES
ACCEPT A VALVE NUMBER
GENERATE GRAPHIC DISPLAY OF VALVE PROGRAM
WAIT FOR USER TO HIT ANY KEY ON TERMINAL
NO
RESPONSE = G ?
YES
INITIALIZE TIME-BASE GENERATOR
WAIT FOR INTERRUPT
INTERRUPT
UPDATE REAL TIME
OUTPUT VALVE SETTINGS TO DACs
RE-ENABLE INTERRUPTS
NO
TIME= RUN LENGTH ?
YES
SHUT OFF ALL DEVICES
HALT
NO
WAIT FOR A NEW RESPONSE



Microprocessor-based system which controls gas flow rates in an epitaxial reactor is comprised of key elements shown in diagram; seven channels of D-A conversion are utilized during this process

tion of the analog output ports limits the number of distinct valve settings to 250 and allows them to be specified all within one byte). Software allows the user to alter entries which were already made during the input process.

After all seven valve programs have been entered, an editor is entered that allows the user to change the run length or any entry in any valve program. A Cromemco D+7A board was used to obtain the seven channels of D-A conversion. The editor prompts "EDIT COMMAND?" and waits for one of four possible responses. The response "R" invokes the routine for changing the run length. The response "V" followed by a valve number causes the enter program for that valve to be listed on the terminal, after which the user may alter, add, or delete entries at will.

If the edit command is "D" followed by a valve number, a bar graph of the selected valve program is generated on the terminal. Columns of asterisks are used to create the bars, and horizontal and vertical axes are labeled to indicate elapsed time and gas flow, respectively. Additional parameters of the program, such as maximum flow rate and number of program entries, are listed along with the graph.

The final edit command is "G." When that command is received, the software initializes and starts a hardwired time-base generator, enables interrupts, and causes a halt. Once each second an interrupt occurs, and the processor enters a service routine that reads each valve program and outputs the appropriate information to the corresponding analog output port. The service routine also keeps track of elapsed time, and when that figure reaches the selected run length, it shuts off all the valves, disables interrupts, and halts the processor. □

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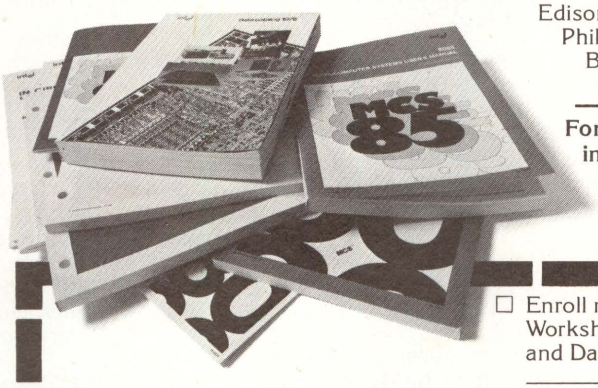
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Montreal, QUE	8/22–26
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MICROCOMPUTER INTERFACING WORKSHOP



September 15, 16, 17, 1977
and
Digital Electronics for Automation Workshop
September 13, 14, 1977
V.P.I. and S.U. Extension Center, Reston, Virginia (Dulles Airport)

Presented by:
The Departments of Chemical Engineering and Chemistry
and
The Extension Division
of
Virginia Polytechnic Institute and State University

Microcomputer Interfacing
COURSE CONTENT

This 3-day workshop will introduce the participant to the basic techniques of microcomputer interfacing and programming and will enable him to proceed on a self-teaching basis toward his own specific applications of microcomputers.

This is a hands-on laboratory course. Participants will use a unique breadboarding microcomputer station that is based on the 8080A-type microprocessor chip and associated support chips such as the 8255 (programmable peripheral interface chip), 8251 (universal synchronous/asynchronous receiver/transmitter chip), and 8212 (8-bit input/output port chip).

Each participant will have an opportunity to use the 8080 family of chips manufactured by Intel, National, Texas Instruments, NEC, AMD, and Zilog. The course should also prove valuable to owners of 8080 kits and microcomputer systems that are currently being marketed by E&L Instruments, Intel, Cramer, MITS, Pro-Log, Control Logic, etc.

Digital Electronics
COURSE CONTENT

This in-depth laboratory/lecture course provides hands-on experience with the wiring of digital circuits of modest complexity involving the popular and inexpensive TTL integrated circuit chip. Several lectures are included that explore current trends in digital electronics, such as digital telecommunications and microprocessors. These lectures point the way to fruitful avenues for continued study in digital electronics.

Upon completion of the course, the typical participant will be able to understand the jargon of digital electronics; read pin configurations from manufacturer's specifications; purchase state-of-the-art integrated circuit chips, hybrid modules, and digital instruments with reasonable confidence; appreciate future trends in digital electronics with an emphasis on microprocessors; and discuss projects with electronics design and instrumentation engineers.

Technical questions should be addressed directly to the course instructors, David G. Larsen, (703) 951-6478, Dr. Peter R. Rony, (703) 951-6370, or Dr. Paul E. Field, (703) 951-5385.

REGISTRATION AND FEE INFORMATION

Pre-registration forms and fees must be received and lodging requests made 10 days prior to the beginning of the workshop.

Registration fee of $145 for 2-day workshop and $195 for the 3-day workshop includes tuition, coffees, administrative costs, and study materials. Make checks payable to the Continuing Education Center, VPI & SU. A request for refund of prepaid enrollment will be honored if notification is received 10 working days before the starting date of the workshop. Attendee substitution may be made at any time. Meals and lodging are not included in the fee. Attendees should make their own room reservations.

WORKSHOP PRE-REGISTRATION FORM

Mail To: Adult Registrar
Donaldson Brown Center for Continuing Education
Virginia Polytechnic Institute & State University
Blacksburg, Virginia 24061 Phone: (703) 951-5182
(Workshops are in Reston, Virginia)

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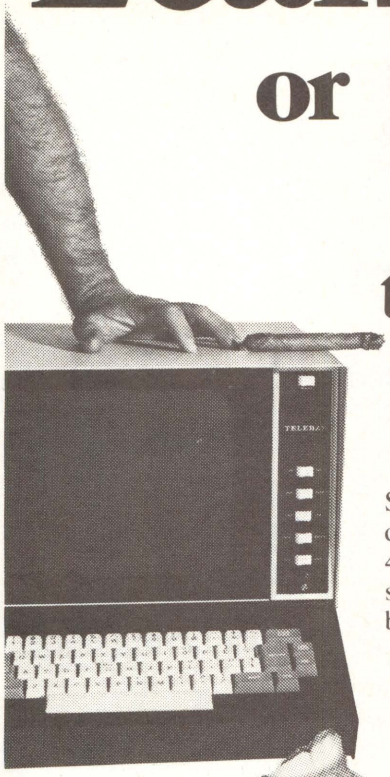
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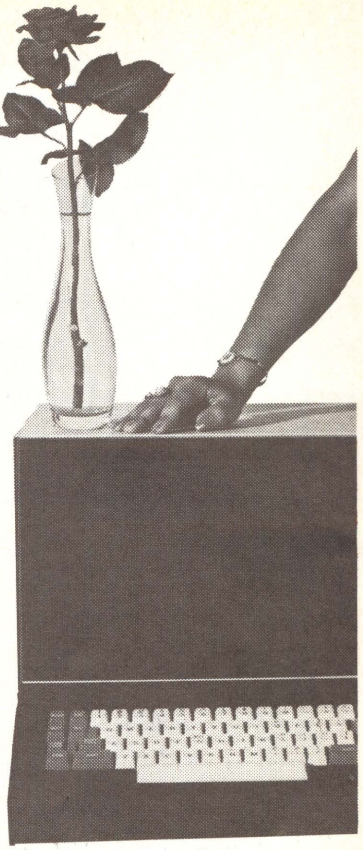
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CIRCLE 96 ON INQUIRY CARD

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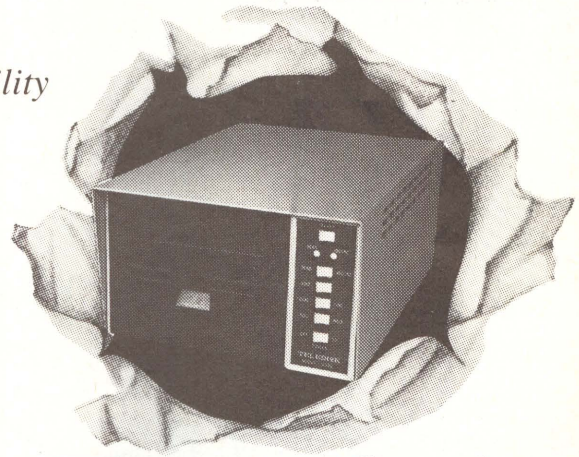
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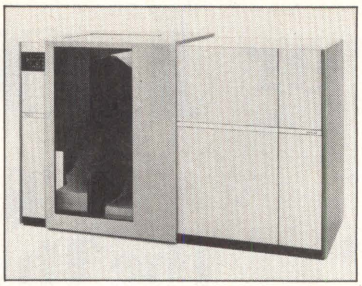
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CIRCLE 52 ON INQUIRY CARD

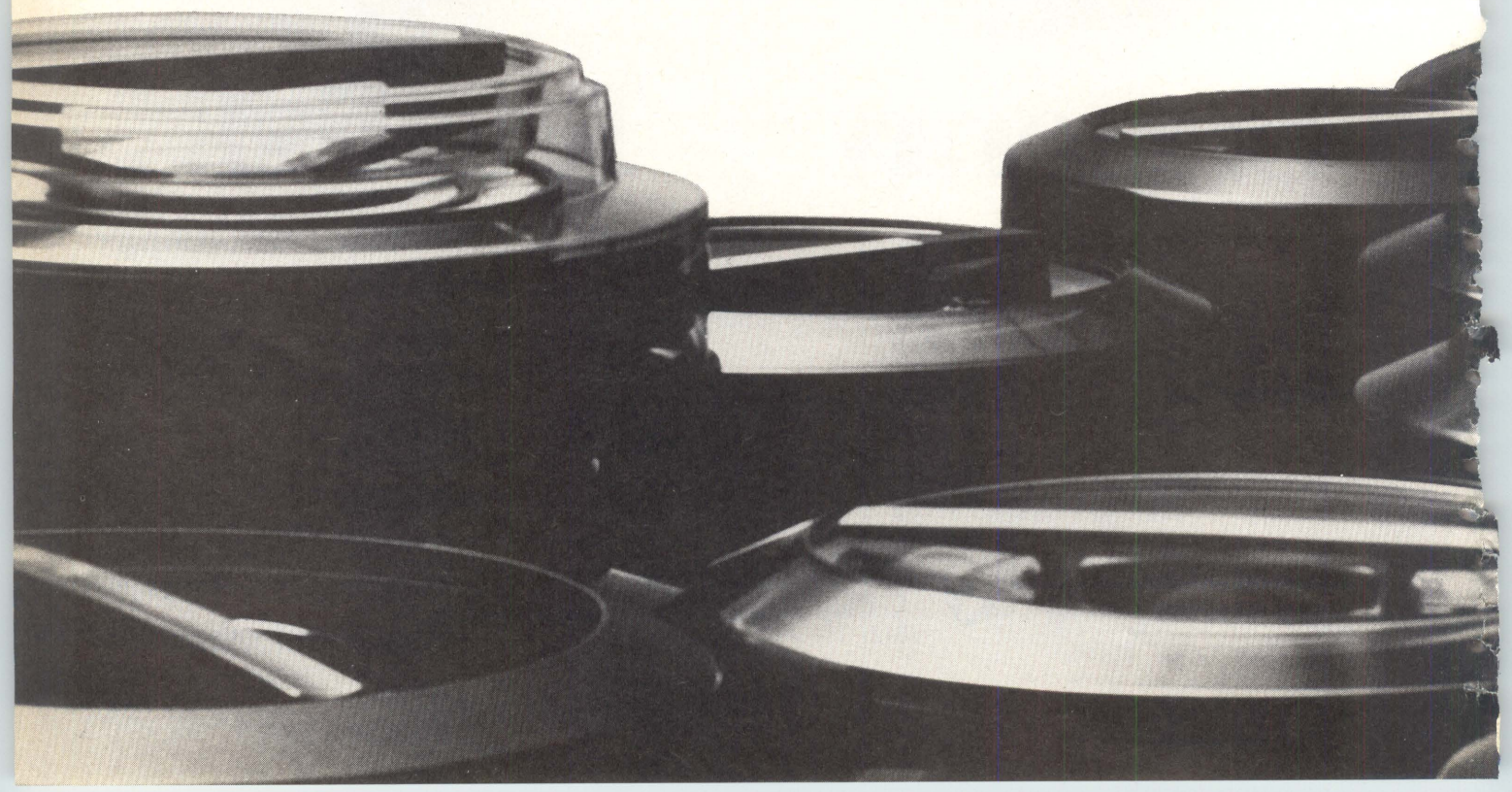
New data-hungry peripherals from Siemens

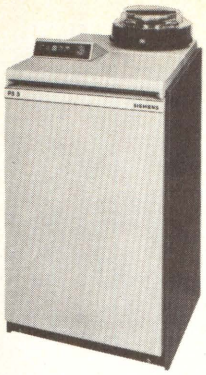
For OEM requirements demanding high throughput from reliable I/O devices, Siemens introduces the data-hungry peripherals.

Siemens ND 2 is the ultimate in hardcopy peripheral systems. It uses a laser and electrophotography to print up to 21,000 lines/min. on plain paper, and outputs approximately 8,800 12-inch sheets/hour. A forms overlay feature, that eliminates the need to preprint computer paper, is available.

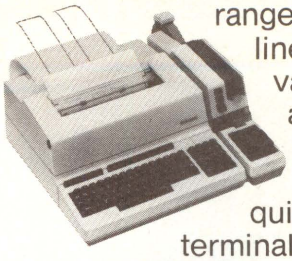


The life of ND 2's photoconductor drum is an unparalleled three million copies...and the drum is user replaceable.





Siemens PS 5 disk storage drive, with an average positioning time of 23 ms, is expandable from 72 to 144 to 300 to 500 MB without cabinetry changes. Users can upgrade easily and your parts inventory stays small. The PS 5 is extremely rugged and reliable with a proven MTBF of 2500 hours, including the first hour of operation. At 500 MB it's the largest capacity disk unit available and the most economical per MB.



The PT 80 terminal features printing speeds of 30 to 90 characters/second and a range of 72 to 132 characters/line. In addition, it offers a wide variety of type faces and the ability to adjust to all common paper sizes.

Its compact design and quiet operation make the PT 80 terminal ideal for use in offices, banks, EDP centers, etc.

To learn more about how Siemens can satisfy your growing data appetite, call or write Richard Mizrahi, Siemens Corporation, 3 Computer Drive, Cherry Hill, N.J. 08034 (609) 424-2400.

SIEMENS

CIRCLE 53 ON INQUIRY CARD





Microcomputer Interfacing: Using Digital-to-Analog Converters

Christopher Titus
Tychon, Inc

Peter R. Rony
Virginia Polytechnic Institute & State University

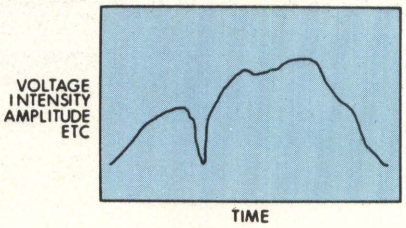
David G. Larsen
Virginia Polytechnic Institute & State University

Jonathan A. Titus
Tychon, Inc

In last month's discussion concerning interfacing of a 10-bit digital-to-analog converter (DAC) to a microcomputer, the memory mapped input/output (I/O) technique was used to transfer data to the DAC. This column will further explore the use of a DAC, showing how it may be used to display data and to generate complex outputs.

A DAC module's analog output generally is used to power or drive some other device, such as a display, stripchart recorder, servomotor, valve, etc. Many analog output waveforms such as a ramp, triangle, or square wave output may be generated under software control using the simple microprocessor increment, decrement, and time delay instructions and routines previously illustrated. These analog outputs are well defined and find application for many of the devices mentioned. Complex outputs may also be needed for special applications.

More complex, nonlinear outputs may be generated in two ways. Software routines may be used to calculate a new value for each point as it is output to the DAC, or may be used to retrieve a new data point from a file of values which have been previously calculated or updated. In last month's software-generated ramp output, it took about 25 ms to generate the 1024-step ramp. Each point was "calculated" as the computer went along; a simple increment instruction, the calculation did not take the computer long. If a longer calculation using software mathematical routines were involved, it might take much, much longer to generate each point. In many applications where data are not output or needed very quickly, this might be acceptable. When data are to be corrected and output to a plotter, the speed of the plotter may be very slow compared with the computer's fast output of data to the DAC. If a calculation is introduced into software, the slow plotter may actually outrun the computer. Calculations of trigonometric functions may take many milliseconds. In some cases it might be better to do the calculations, store the results, and then output the data as a file.



Typical complex output well suited for microcomputer/DAC display

Some controllers and experiments may either generate or require complex waveforms for which no simple formula exists. In these cases it may still be desirable to display or generate information using the DAC module. The following example illustrates how software and a DAC are used together to display a file of data. We have chosen to use accumulator I/O instead of the memory mapped I/O technique shown in last month's Fig 1. The only change necessary is to use OUT instead of the MEMW signal shown. Now OUT instructions are used to transfer the data to the holding registers within the DAC.

When using an oscilloscope to display data, it is necessary to refresh or update the display. If data are output only once, we would miss it since our eyes cannot respond very quickly to the single trace. It is necessary for software to detect the end of the data file and, when this point is reached, start the display again. The software for a file

Note: Two workshops to be directed by Dr Peter Rony, Dr Paul Field, and David Larsen have been scheduled. "Microcomputer Interfacing Workshop," Sept 15-17, is based on the 8080 microprocessor, providing over 20 operating 8080 computers for participant use. A 2-day workshop on Sept 13 and 14, "Digital Electronics for Automation" centers on small- and medium-scale TTL ICs. In-depth lectures will be supplemented by laboratory time with individual breadboarding stations. Both sessions will be held at the VPI & SU Extension Center in Reston, Va (Dulles Airport). For further information, contact Dr Norris Bell, VPI & SU, Blacksburg, VA 24061, tel: (703) 951-6328.

Typical Software For a 100-Point, 10-Bit DAC Display

```
                                *000  000
000  000  041      START,        LXIH        /Load H & L with memory pointers
000  001  000                    000         /LO address pointer
000  002  005                    005         /HI address pointer
000  003  323                    OUT         /Generate trigger pulse
000  004  007                    007
000  005  176      AGAIN,        MOVAM       /Get the first point
000  006  323                    OUT         /Output eight LSBs
000  007  004                    004
000  010  043                    INXH        /Increment the memory pointer
000  011  176                    MOVAM       /Get the second part of the word
000  012  323                    OUT         /Output two MSBs
000  013  005                    005
000  014  323                    OUT         /Strobe the DAC
000  015  003                    003
000  016  175                    MOVAL       /Move L to register A
000  017  376                    CPI         /Compare it to the data byte
000  020  310                    310         /310 = 200 decimal
000  021  302                    JNZ         /Done all 100 points?
000  022  005                    AGAIN       /No, do the next point by jumping
000  023  000                    0           /to again
000  024  303                    JMP         /Yes, jump back to start to do
000  025  000                    START       /it all over again
000  026  000                    0
```

of data stored in memory (see the Program) will display 100 data points over and over again. (The assembly language format shown is that of the resident editor/assembler developed by Tychon, Inc for 8080 systems.) The data file starts at address 005 000 and goes to 005 310. Data are stored as:

Location X	Eight Least Significant Bits	D7-D0
Location X + 1	Two Most Significant Bits	D1-D0

The six remaining bits in the second data word, D7-D2, are not used and are ignored by the DAC. An OUT 007 command has been added to the software to signal the start of another scan through the 100 data points. The pulse generated by the OUT 007 command through external decoders is used to *trigger* the oscilloscope to start a new scan. This is an important feature; without it there would be no way of telling where the 100 data points started or ended. We would only see a display of the 100 points again and again with no reference point, much like the display of a sine wave.

This technique is particularly useful for displaying data which have been already acquired from an instrument; it is also very useful when generating a well-defined waveform to simulate an instrument's output or to provide an output for testing a piece of equipment. Many devices have outputs which are voltage dependent, such as servomotors, power amplifiers, and voltage-controlled oscillators. In many cases it is important to provide these devices with a standard test output. To generate an output such as the one in the Figure would be difficult using standard signal generators or even the available function generators. It is relatively easy using a microcomputer and a DAC. The test pattern of interest is stored as 10-bit values in a p/ROM and is accessed by a program similar to the one just used. This procedure will output the waveform to our instrument. With variations in software it could be output only once, five times, or any other number of times. Time delays could also be introduced between points to slow down the output. The highest speed is fairly well fixed by the computer's execution time. The 100-point program will output data at about one point every 22 μs or 2.2 ms per pass through the file. This assumes a 1.3-μs clock period.

It is important to note that the output from the DAC still consists of discrete steps; it is not continuous. A close look at the scope output will show this to be true. If a real, continuous output is needed, some filtering or integration may be required. Such considerations are beyond the scope of this column, but filtering techniques have been discussed elsewhere.*

Just as several programs and subroutines may be stored in ROM or p/ROM in the computer's memory, so too, many possible data files may be stored for later use. In some applications, it may be necessary to store simulated outputs from many instruments or a series of analog correction values to be output to a DAC module. In doing so, we have again substituted some software for hardware. The p/ROMs and display software have been substituted for complex waveform generators. More flexibility is probably available in software than in hardware-only solutions to the problem; however, we are limited by the computer to a rather slow output.

*G. E. Tobey, J. G. Graeme, and L. P. Huelsman, *Operational Amplifiers, Design and Applications,* McGraw-Hill Book Co, Inc, New York, 1971

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Magnetic Card Reader/Writer Employs 4-Stripe Plastic Card Programming Medium to Store 1k Bytes

The combination of the series KB-31 Microloader and Kilobyte Card, designed for low cost indoor or outdoor program loading, field program modification, and user-actuated diagnostics, has been introduced by Vertel, Inc, 167 Worcester St, Wellesley Hills, MA 02181 as the first such reader/writer and 1024-byte magnetic card medium. The reader/encoder will record and read both channels per stripe on the 1024-byte (8-bit) magnetic stripe card, with a character load time of 5k bytes/min. The company's proprietary recording technique allows for substantial increase in effective bit density without significantly altering the magnetic flux reversal density defined in the ANSI standard for credit cards.

Measuring 3.2 x 8.19 x 2.48" (8.2 x 20.8 x 6.3 cm), the reader/encoder features a diecast frame and chassis, and a constant-speed governed motor. Precision tracking magnetic head travels along a highly accurate lead screw running in shielded ball bearings, and is guaranteed for 500,000 operations.

Stationary case design, with enclosed fully-gimbaled moving read/encode head, minimizes errors, data loss, damage, or jamming due to card warpage, thickness variations, and foreign material. In addition, the unit cannot operate unless the card is properly inserted.

The device records and reads two channels/track, simultaneously and independently. Typical recording densities are 528 fr/in (20.8 fr/mm). Channel 1 uses ANSI-standard "F2F" credit card coding; channel 2 uses "4F" coding. Data block or track length is 2.81" (71.4 mm) typical for ISO/ANSI standard. Read speed is 3.5" (89 mm)/s.

The Kilobyte Card has four stripes, with two channels encoded on each. The durable plastic card is smaller, lighter, more efficient, and less costly than other media currently available for program or data storage.

Contending media (in the games market) include floppy discs, tape cassettes, tape "wafers," audio records, calculator data strips, and ROMs. Providing performance needs for programmable video games, floppy discs represent an overkill in terms of storage capacity, speed, and cost. With similar problems, tape cassettes are also prone to dropout errors. They suffer from reliability and data integrity problems, as do the miniaturized versions which are less expensive.

Cartridges (tape wafers) use a less expensive reading mechanism. However, they suffer from major reliability problems and may snarl internally. Forty-five r/min discs can be recorded with several programs, but a record player must then be added. The discs are susceptible to fingerprints, dust, and wear, which could lead to program errors. These same problems affect calculator data strips which carry only a maximum of 200 bytes. Comparable in cost to magnetically striped cards, the strips require motorized readers.

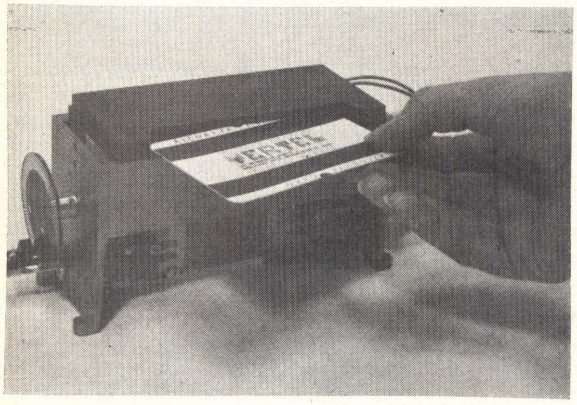
ROMs require no electromechanical reading devices or internal memory. They do, however, experience connector failures, limiting the number of insertions. Another problem is the enormous consequences of program bugs. With ROM cartridges, the major drawback is price.

Programs in BASIC have already been encoded onto the cards—for use as an input media for a microprocessor-based computer. In addition to games, cards are used to program a computer with calculator routines.

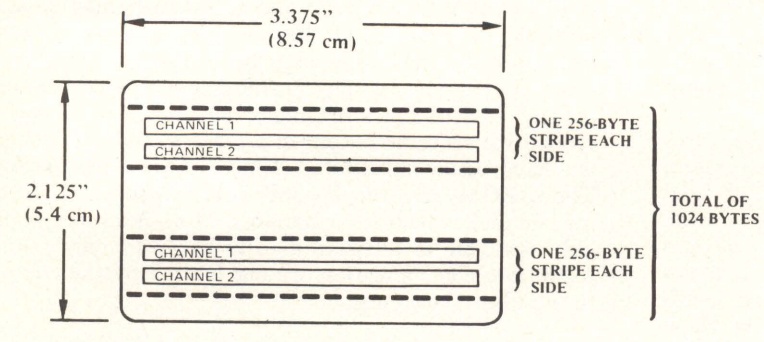
Four electronics options are available with solid-state motor control electronics. Option 1 is self-synchronizing flux reversal output, TTL; 2 is unbuffered eight bits parallel-plus-strobe output; 3 is buffered microprocessor common bus output; and 4 is buffered RS-232 output, with choice of 12 V, TTL, or 20-mA current loop.

OEM prices for the Microloader are $99 without read/write electronics, or $258 complete, in 1000 quantities. Kilobyte Cards typically cost $0.10 each in large quantities.

Circle 170 on Inquiry Card

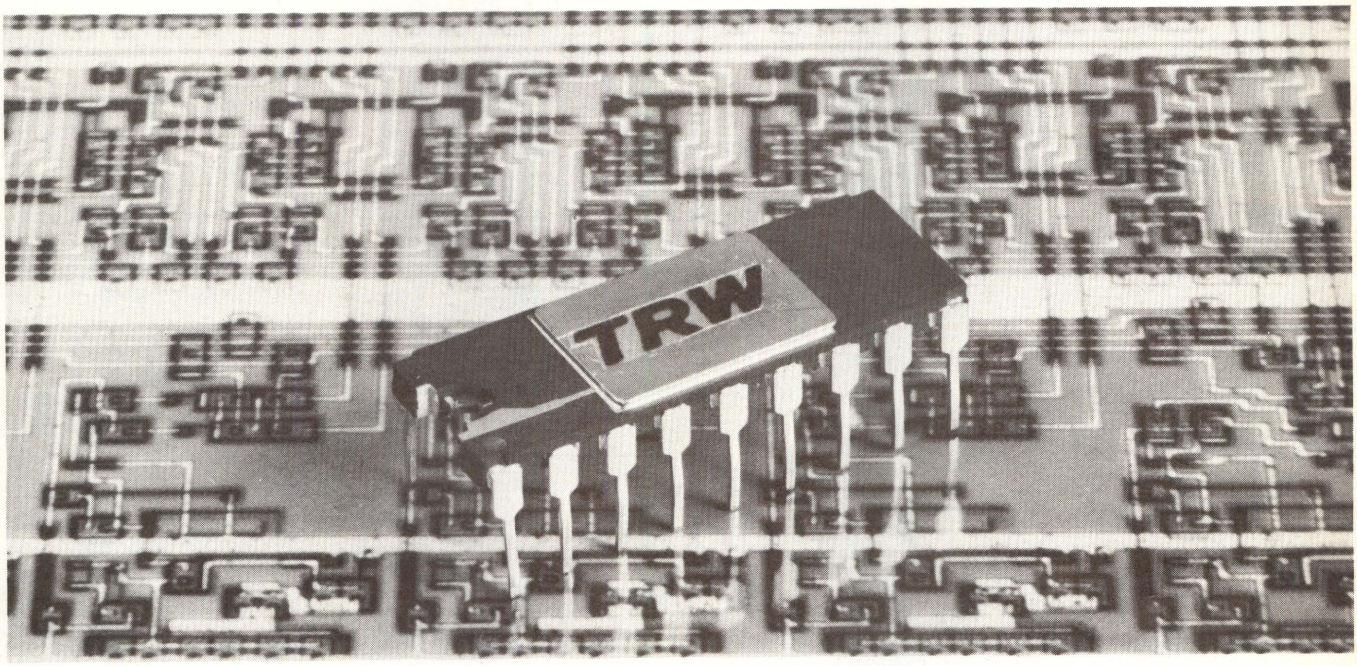


Designed for microprocessor-based programming aplications, Microloader magnetic card reader/encoder from Vertel records and reads two channels/track, simultaneously and independently, from 4-track Kilobyte Card inserted into unit. Technique increases effective bit density without changing flux reversal density



Same size as a standard credit card, Vertel's Kilobyte Card stores data on four magnetic stripes, each with two channels. It is less costly and more efficient than other media currently used for program or data storage

8-Bit high-speed monolithic A/D



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CIRCLE 54 ON INQUIRY CARD

Z80 In-Circuit Emulator Provides Powerful Hardware/Software Tool

Comprised of a single trace/emulator board, totally bus and software compatible with the MDS 800, together with a processor pod, user control software, and direct, isolated connectors to the prototype socket, Z80 ICE® is claimed by Relational Memory Systems, Inc, PO Box 6719, San Jose, CA 95150 to be the only emulator to provide electrical and timing identity with the Z80A at the user socket, along with BREAKREGION® and page memory mapping. It is the only available alternative to the Zilog ICE on the market.

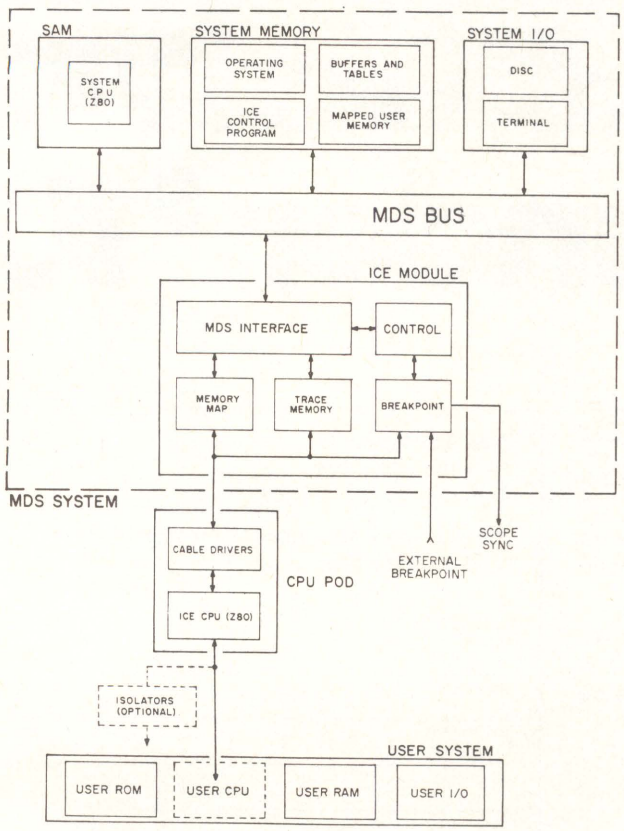
This microcomputer subsystem communicates with the Intellec® MDS-800 8080 central processing module or with the company's Z80/MDS MCB® via shared memory and I/O commands through the MDS-800 universal bus. With the emulator, the MDS-800 can be used to develop and debug products based on the Z80 CPU.

Hardware and software features include the Z80 CPU mounted on an external pod close to the prototype; RAM-based software; and continuous refresh of prototype memories. Wires from the pod provide an external oscilloscope signal, enable triggering a break, and allow substitution of a clock signal for the prototype clock. Oscilloscope synchronization pulse and external break signal are provided at the pod. Memory mapping permits substitution of 4k-byte pages of MDS-800 system memory for prototype memory. Other features are multiple master bus control logic with bus lockout, hardware memory protect, and trace memory.

The device is operated by a control program resident in MDS main memory, by sharing memory and bus resources between the host processor and Z80 ICE. Software is an Intellec system program, providing the user with a large, powerful command repertoire that permits flexibility in describing operations. One version is for the standard MDS-800 system with the 8080 CPU and Intel monitor; a more powerful version is for MDS-800 systems using the company's Z80 system adapter module.

A generalization of the breakpoint concept, BREAKREGION permits the user to define regions in memory or I/O address space in which breaks are to be made in emulation. This ability to close in on hardware or software faults facilitates debugging. Break conditions are formed from logical assertions of the Z80 CPU lines. Also permitted with the emulator are two independent user-defined break conditions, one manually activated break switch, one externally activated break, and one oscilloscope sync pulse line.

Circle 171 on Inquiry Card



In-circuit emulation module from Relational Memory Systems for Intellec MDS-800 and company's Z80/MDS MCB features memory mapping, trace memory, external pod to mount the prototype, and BREAKREGION debugging concept

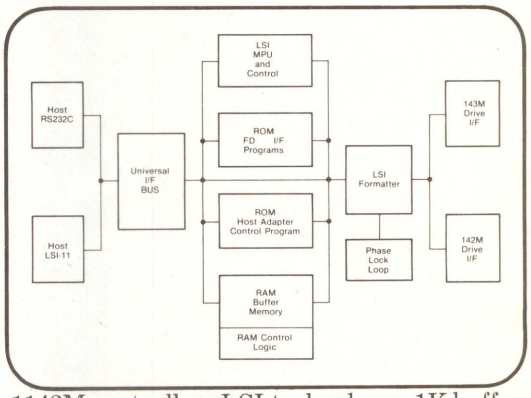
Bipolar PACE CPU on Single Board Features More Power

Combining the minicomputer-like architecture of the PACE with features of single-board units, the Super-PACE single-board bipolar device is 30% more powerful than some minicomputers and two to two and one-half times more powerful than many other single-board microcomputer systems. This high speed Schottky TTL enhancement of the 16-bit p-MOS PACE microprocessor from National Semiconductor, 2900 *Semiconductor* Dr, Santa Clara, CA 95051 features an expanded set of 75 instructions; it is also source-code compatible with the complete PACE family. It is expected to fit into applications be-

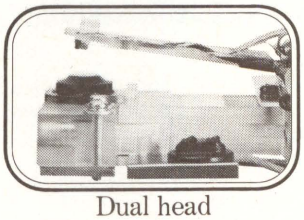
Meet the First Family in floppies.



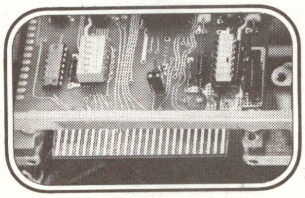
The roots of our floppy family



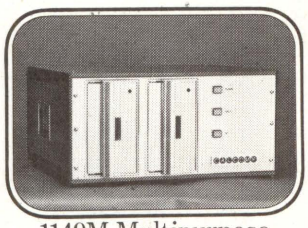
1143M controller • LSI technology • 1K buffer



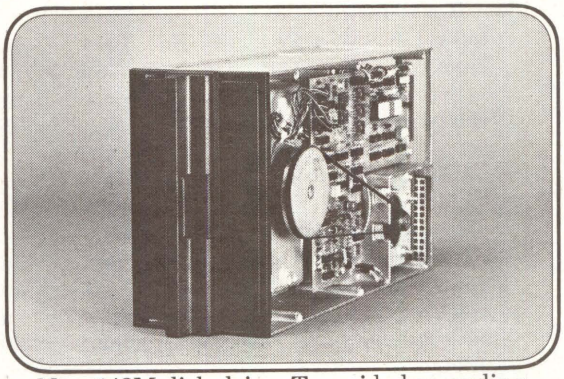
Dual head



50 pin LSI interface



1149M Multipurpose
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Rack or table mounted.



New 143M disk drive. Two-sided recording.
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LSI-11
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tween the n-MOS single-board microcomputers and bipolar slice-oriented minicomputers.

The microprogrammed Super-PACE board features a 16-bit address bus and separate 16-bit bidirectional data bus, implemented with 80 bipolar Schottky MSI chips. The processor portion consists of eight 64-bit edge-triggered registers, four 16-bit binary arithmetic logic units, and two Tri-State™ 8-bit universal I/O shift registers.

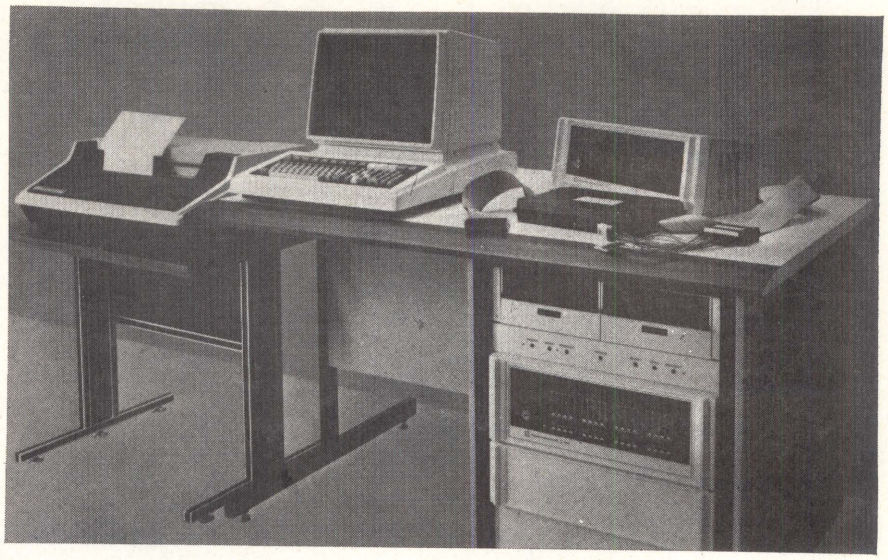
In addition to an onboard clock generator, the timing and control portion of the board contains eight 2k-bit bipolar ROMs for microprogram storage, seven to ten decode ROM packages, and five to seven Tri-State counters for microprogram address control. Another 40 to 50 chips perform I/O control, address register, and I/O data buffer functions. Built-in bus request logic permits implementation of data transfer synchronization and external bus controllers.

The 8.5 x 11″ (21.59 x 27.94 cm) CPU board, IPS-16C/100 features a 220-ns cycle time and average instruction execution interval of 1 μs. Other typical instruction execution times are 1.1 μs for logic and arithmetic, 1.05 to 1.27 μs for stack, 660 ns for register data transfer, and 880 ns to 1.06 μs for load or store memory transfer. CPU boards are priced from $529 to $600 each in 100 to 1000 units; price of single units is $831.

Support includes a line of memory and peripheral boards as well as software and programming aids. A 6-slot prototyping system incorporating the CPU board, 16k x 16 RAM board, 8k x 16 p/ROM board, I/O communications interface board, and software package is available for $3735.

Flexible Microprocessor Development System Gives 9900 Design Support

The floppy disc-based microprocessor development system combines high performance with low cost flexibility to provide comprehensive hardware and software design support for users of the TMS9900 series microprocessor. The system provides emulation support with logic state analyzer development capabilities.



Emulation support and logic state analyzer development capabilities are dual functions of FS 990 microprocessor development system from Digital Systems Div of Texas Instruments. Desk-based system includes 990 microcomputer, dual floppy disc drives, video display terminal, and optional printer

Texas Instruments Inc, Digital Systems Div, M/S 784, PO Box 1444, Houston, TX 77001 has based the system on the FS990 software development system. The microprocessor development system features TMS9900 microprocessor emulation, logic state trace, p/ROM/ROM implementation, FORTRAN, and AMPL (Advanced Microprocessor Programming Language). These characteristics enable software development in both FORTRAN and assembly language, integrated software/hardware emulation for debug and test, and firmware implementation.

Emulation feature provides support during the entire design phase. Logic state trace includes up to 20 channels of general-purpose TTL signal trace with four channels available for glitch latch (spike detection). Sampling rate is to 10 MHz, with glitch detection for pulse widths down to 10 ns. Four control probes allow qualifying trace sampling conditions.

The p/ROM/ROM implementation support includes the capability to generate industry-standard BNPF and high/low formatted output. EPROM or p/ROM devices can be generated inhouse with the 990 p/ROM programming unit.

FORTRAN includes higher level language support for tasks to be executed within the host system. An additional feature is the generation of standalone routines in FORTRAN, which can be compiled to 990 computer object code for execution on a 9900 target system.

Emulation and trace modules are controlled from the company's model 913 video display terminal by AMPL, an interactive high level programming and control language. It unifies prototyping capabilities into an integrated system, simplifying orientation for the beginner, while providing extensive versatility and support for the experienced user.

The desk-based FS990 system includes a model 990/4 microcomputer with 24k words of 16-bit memory, dual floppy disc drives, and the video display terminal. Options include the p/ROM programmer, Trace Data Module Kit, model 810 printer, and FORTRAN software license. Basic system is priced at $13,600.

Circle 172 on Inquiry Card

Bipolar Microprocessor Is Suited to Military Applications

The 8X300 high speed monolithic microprocessor with a fixed instruction set has been found to suit many applications in military, airborne,

Switch to the oem line printers that can cut your customer's paper cost 30%.

ABCDEFG
ABCDEFG ← compressed pitch is the secret →

Ask Control Data.

Users are already specifying Control Data's exclusive Band Printers with compressed pitch capability! And it's easy to see why.

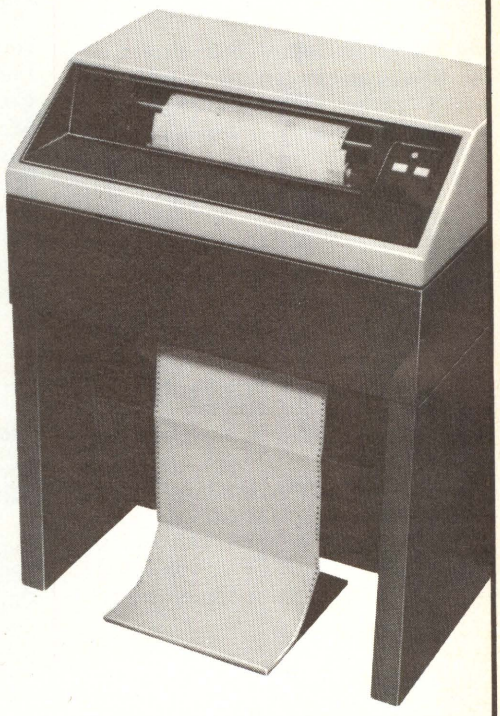
This breakthrough in horizontal font technology can cut their paper requirements 40% . . . paper cost 30% . . . and paper storage cost dramatically.

With its standard 10-character-per-inch band, the Control Data Band Printer creates standard-size printouts. But after a simple 30-second switch to our 15-cpi band, it can actually print a solid-stroke 132-character line on a letter-size sheet! Or 204 characters on 14⅞″ wide paper. The printer adjusts to either pitch automatically. What's more, you can offer a paper-saving choice of 6 or 8 vertical lines per inch!

Don't miss this opportunity!

Control Data Band Printers are available through OEM suppliers only. Our 300 and 600 lpm models offer the exclusive compressed-pitch feature; our 900 lpm the standard 10-cpi bands. Between all three look-alike models, there are only six minor differences. Identical spare parts kits offer a choice of speed, without committing capital to a mountain of spares.

So go ahead of competition. Offer your customers the printer that can cut their paper cost 30%. Not just a promise for the future . . . but a product available through OEM's today!



Phone (313) 651-8810 or write: Harrison Craig, Product Sales Manager, Control Data Corporation, 1480 N. Rochester Road, Rochester, Michigan 48063. ☐ Ask a CDC Sales Representative to bring me a Band Printer evaluation unit. ☐ Send more information and sample print-out.

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CONTROL DATA CORPORATION

CIRCLE 56 ON INQUIRY CARD

and space environments. Such uses include missile and airborne controllers, data communications, terminals, bus translators, power control systems, and real-time processors.

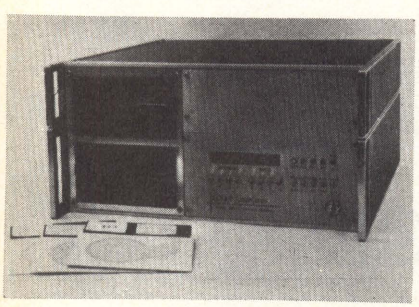
Introduced by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086 (see *Computer Design*, "Micro Processor/Computer Data Stack," Nov 1976, pp 150, 152), the device utilizes bipolar Schottky technology to achieve the necessary performance over the full military temperature and voltage ranges. The process inherently yields radiation hardened circuits; tests for radiation effects are planned by a user. The unit operates from a single 5-V power supply which can be strobed in extreme environments and under tight system constraints.

Circle 173 on Inquiry Card

Microcomputer Features Dual Minifloppy Drives for Software Development

The dual minifloppy disc drives of the GNAT-PAC system 8 microcomputer, together with complete system software, enable development and debugging of extensive production software. Providing increased versatility, the minifloppy drives have storage capacity of 80k bytes of formatted data in single density. The 8036 module interfaces to the system using the FD 1771 disc controller chip. Operations feature onboard data buffering, automatic seeking, disc initialization, IBM soft-sectored format, and automatic motor shutoff between extended access.

GNAT Computers, Inc, 7895 Convoy Ct, Unit 6, San Diego, CA 92111 has equipped the extended system with a 1.3-μs 8080A CPU, 16k RAM, 2k p/ROM on 16k module, serial/parallel I/O, disc interface and controller, and hexadecimal front panel in six of the 12 chassis slots. Additional memory and I/O modules are available to meet specific application needs.



Included with the system, which is priced at $3690 in single units, are a monitor, bootstrap loader, and disc operating system, as well as a complete file manager, console commands, peripheral interchange, load, dump, and submit. PLM, BASIC, FORTRAN, and other high level languages are available.

Circle 174 on Inquiry Card

High Performance Slice Covers Both Commercial and Military Ranges

Pin-for-pin and functionally compatible with the standard 2901, the 2901A 4-bit microprocessor slice is a high performance version, specified to be 20 to 30% faster over both commercial and military temperature ranges. The devices from Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94040 feature lower guaranteed power dissipation at elevated temperatures and higher drive capability on Y outputs. The 100-piece prices are $14.70 (commercial) and $83 (military).

Circle 175 on Inquiry Card

General-Purpose µComputer Encompasses Z80 Characteristics

Capitalizing on the features of the Z80, Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 has designed the MCS microcomputer as a self-contained general-purpose unit which makes use of the full 158-instruction set. This set includes 4-, 8-, and 16-bit operations, and BCD arithmetic and shifting capability. The 8-bit CPU directly supports both bit and string data.

With 600k bytes of dual floppy disc storage, the system can address 64k bytes of main storage. It has an RS-232 or current loop serial interface for use with a CRT or TTY, and standard busing structure. Support modules include additional parallel and serial I/O channels, RAM and ROM, and wirewrap boards for special interfacing.

Components of the basic system include a disc controller, 16k bytes of dynamic RAM, and 3k bytes of p/ROM containing a system debugger, floppy disc driver, console driver, and bootstrap routines. Located in the disc drives are an MCS executive, ZDOS operating system, an editor, macro assembler, and file maintenance software programs. A linking loader and relocatable assembler are optional, as are BASIC, MCS-RIO, and soon to be available MCS-COBOL.

Circle 176 on Inquiry Card

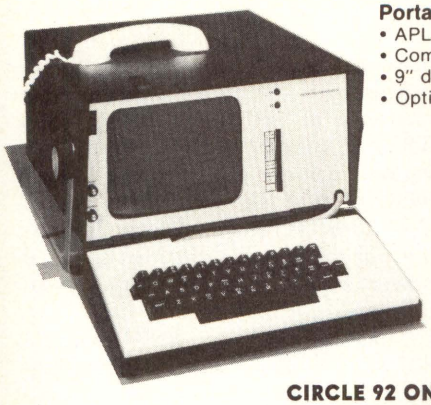
Powerful Microcomputer Development Center Is Three Systems in One

The Intellec® 888 System, an enhanced version of the MDS 800, is claimed to be the most powerful microcomputer development center available. It has two to four times the online storage capacity of other systems, which expedites applications programming.

As three systems in one, the basic device contains all software and hardware resources necessary to develop software in assembly language or PL/M-80™ high level compiler language for the 8085 microcomputer system, the 8080 system, and the SBC 80 family of OEM computer systems. With the addition of an optional macro assembler to the resident system software, it can be used to develop software in assembly language for 8048, 8748, and 8035 single-chip microcomputer systems.

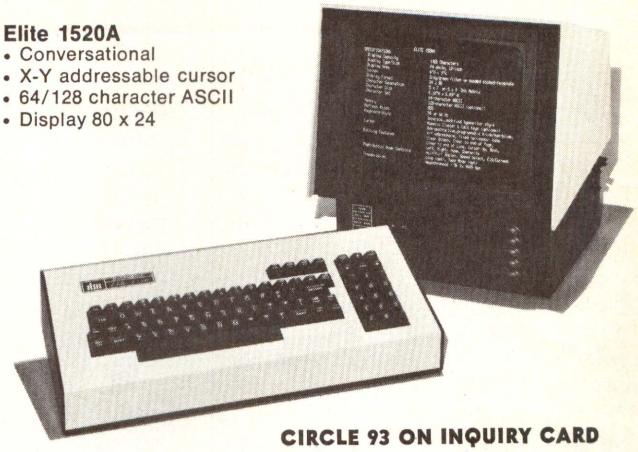
Introduced by Intel Corp's Microcomputer Systems Div, 3065 Bowers Ave, Santa Clara, CA 95051, the basic package includes diskette system; MDS 800 system; CRT display console; PL/M compiler for the MCS-80™ and -85™, SBC 80, and system 80; and diskette operating system. A 1M-byte diskette system contains two double-density drives, each of which stores 0.5M bytes of data in soft-sectored format. The intelligent controller is implemented with the company's series 3000 bipolar micro-

See things your way



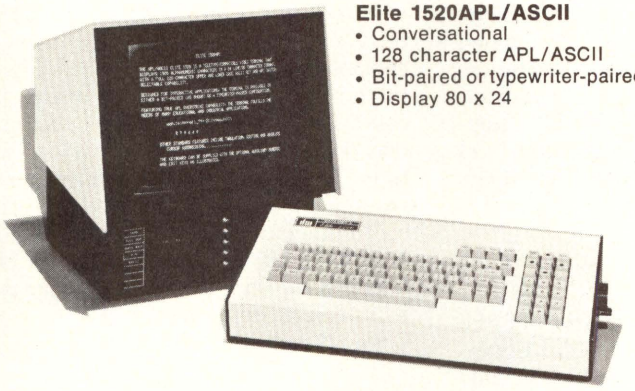
Portable Elite 1520A
- APL/ASCII (optional)
- Compact, rugged construction
- 9" display
- Optional acoustic coupler

CIRCLE 92 ON INQUIRY CARD



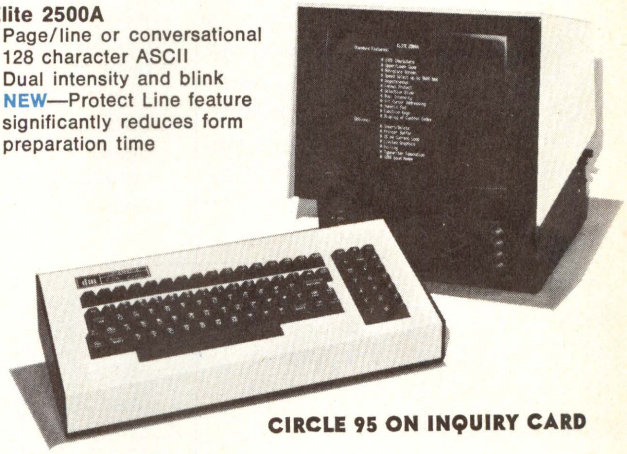
Elite 1520A
- Conversational
- X-Y addressable cursor
- 64/128 character ASCII
- Display 80 x 24

CIRCLE 93 ON INQUIRY CARD



Elite 1520APL/ASCII
- Conversational
- 128 character APL/ASCII
- Bit-paired or typewriter-paired
- Display 80 x 24

CIRCLE 94 ON INQUIRY CARD



Elite 2500A
- Page/line or conversational
- 128 character ASCII
- Dual intensity and blink
- NEW—Protect Line feature significantly reduces form preparation time

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A family of video terminals that offers a wide range of features to perform an even wider range of data entry and display tasks.

If you're with an OEM firm or a system house, and look at peripherals with one eye on cost and the other on performance, you'll want to take a long look at these proven products from Datamedia.

Their modular design makes troubleshooting a breeze, and facilitates conformance to your system needs, and their quality workmanship assures that those needs will be met longer than you thought possible.

And if you believe in service after the sale the way Datamedia does, you'll appreciate the new dimension we've given to the word "responsive."

Datamedia. We've been seeing things the right way for users in industry, business services, government, education, medicine and research around the world.

Why don't you see what we can do for you.

NEW!



Elite 4000A Programmable Terminal System
- Microprocessor based
- Direct memory access
- Expandable display memory
- 8-level video

CIRCLE 57 ON INQUIRY CARD

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5456 McConnell Avenue • Suite 180 • Los Angeles, CA 90066 • 213-397-3556

Canada: Datamex, Ltd., Ontario/Quebec • **Belgium:** Inex, (02) 512 4037 • **Finland:** Suma, (90) 440391 • **Italy:** Eltron s.r.l., (030) 55-26-41554 • **Sweden:** Teleinstruments ab, 08-38 03 70 • **Switzerland:** Teledynamics, 01-56 3300 • **United Kingdom:** Mellor Data, 020629-8181 • **West Germany:** Video Data Systems GmbH, (0 61 81) 7 39 51 • **Australia:** Intelec Data Systems, (03) 232-3118 • **Japan:** Protech, Inc., (03) 384-0225.

computer set. Addition of a second drive unit expands the system to 2M bytes. Files totaling 1.75M bytes can be created and used online. Programs from the company's user library will be available on diskette as further support.

The Intellec MDS 800 system includes 64k bytes of RAM, CPU, system monitor, peripheral interfaces, diskette controller, system bus, and front panel controller. The system monitor resides in ROM; bus system includes an 8-level priority arbitration network, allowing the system to develop multiprocessor microcomputer systems. The interactive CRT is teleprinter-compatible with a detachable keyboard. It provides access to hardware and software resources and supports debugging with ICE modules. Features include asynchronous data rates to 9600 baud, and cursor positioning and homing. Data can be printed out on the compatible Intellec line printer.

The resident PL/M compiler runs under the ISIS-II (Intel Systems Implementation Supervisor) diskette operating system; it performs all file management tasks. Components are text editor, relocating macro assembler, linker, loader, and Library Manager™.

The development system is compatible with Intellec ICE™ modules and peripherals. Optional units allow the system to be used for microcomputer system prototyping, software/hardware integration and debugging, field testing, production testing, and system documentation, as well as for software development. Basic system is priced at $13,390; optional macro assembler at $300; and optional second diskette unit at $3350.
Circle 177 on Inquiry Card

Industry Standard Interface Links Together Up to 15 Instruments

Conforming to IEEE standard 488-1975 for programmable instrumentation, the IBV11-A interface is contained on a single PC board assembly that plugs directly into any LSI-11/PDP-11/03 bus-structured system backplane. The device can connect up to 15 instruments to the microcomputer. It can also communicate with another identical interface, permitting links between LSI-11s.

The instrument-bus portion of the interface developed by Digital Equipment Corp's Components Group, One Iron Way, Marlborough, MA 01752 will support a total cable length of 65.6 ft (19.99 m), and is hardware-compatible with any system using the LSI-11 as a component. Devices connected to the instrument-bus side act to control functions, send data to the computer, or receive commands from the computer. Operation is through conventional LSI-11 software protocols.
Circle 178 on Inquiry Card

Additions Include Modular μComputers and System With Logic Unit

Supplementing the SAB 8080 microprocessor system, the SAB 8085 contains a complete logic unit with clock generator and system control on a monolithic base, as well as arithmetic unit and working registers. Both are fully software compatible. Seven programmable devices for this microprocessor have also been announced by Siemens Aktiengesellschaft, D-8000 München 1, Postfach 103, Munich, Germany. They can be used as memories (256-byte static RAM, 2k-byte ROM—also erasable), or can control floppy discs, data transmission, terminals, panels, and displays.

The SAB 8048 modular single-chip microcomputer incorporates not only the arithmetic/logic unit and a 64-byte RAM, but also a 1k-byte ROM, 27 programmable I/O ports, and a timer on the one crystal surface. It is available in mask-programmed and erasable user-programmed versions, with or without a ROM. Also included in the family are memory and I/O expanders.

A further modular microcomputer system, SMPE80 is also based on the 8080 system. It is supplied on plug-in boards with customary European dimensions of 160 x 100 mm (6.3 x 3.9"). It comprises I/O modules and various memory units (up to 4k-byte EPROM and 1k-byte static RAM). Test adapters, etched backpanel wiring, packaging systems, plugs, and power supply units have also been developed for the system.

Modular development systems SBC 8010 and 8020 are contained on plug-ins complying with American standards. User programs can be developed rapidly and without delay on preproduction series equipment.

Based on the SBC 8010, the SYS 8010 microcomputer is ready to use, enclosed in a metal case. In addition to the basic microcomputer board, it contains power supply, ventilator, and start program. The system is fully compatible with teleprinter equipment and peripheral equipment conforming with interface standard RS-232-C. Boards for expansion of memory capacity and for series-parallel interfaces are also offered.
Circle 179 on Inquiry Card

Open-Frame Power Supplies Drive 8080A Microprocessors

Designed to drive a wide range of microprocessors, including the Intel 8080A, the MP series of open-frame supplies holds regulation problems to a minimum in order to keep the systems running smoothly. Line regulation is held to 0.1% 5 mV NL-FL; in the case of load regulation, devices offer ±0.1% 5 mV for a ±10% input change.

Ripple is kept to 2 mV rms max, 20 mV pk-pk max. Remote sensing terminals maintain regulation at the load, compensating for up to 0.25-V loss in the load cables. Transient response is 50 μs.

Announced by ACDC Electronics, a div of Emerson Electric Co, 401 Jones Rd, Oceanside, CA 92054, MP301 and 401 each provide three outputs isolated from line and ground. The 301 offers 5 V at 3 A, 12 V at 0.5 A, and −5 V at 0.85 A; 401 provides 5 V at 6 A, 12 V at 1 A, and −5 V at 1 A. All current ratings are at 40°C, derated linearly to 50%

Now, Intel delivers memory for PDP-11/04 and PDP-11/34.

Intel is now shipping high speed, low cost memory for two of the hottest new minicomputers, DEC's PDP-11/04 and PDP-11/34.

That means you can get 30-day delivery and 30 to 50% savings by specifying Intel, the largest independent manufacturer of semiconductor memory.

We can give you add-in memory and add-on memory, both totally compatible with PDP-11 hardware and software. Our in-4711 is an add-in memory for the PDP-11 family and slides into an available memory slot, without modifications. For add-on memory capacity, simply attach the in-4011 memory system. You can add memory in 16K x 16 bit increments, up to 128K words.

Built with the proven Intel 2107B 4K RAM, the in-4711 memory is fully transparent to the CPU, with greater processing speed. For maximum throughput you can interleave two memories.

The in-4711's lower power consumption permits wider operating margins on the main frame power supply and results in a cooler running, more reliable system.

If you've picked DEC to be your computer supplier, go with the best for memory, too. Intel delivers a complete line of add-in and add-on memory for the entire PDP-11 family.

That puts two good names together. Add a third —yours— with the coupon.



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CIRCLE 58 ON INQUIRY CARD

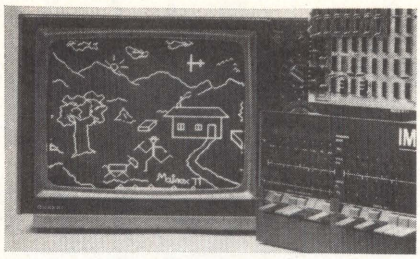
at 70°C. Inputs on both are 105 to 125 Vac, or 210 to 250 Vac. Operation is at 47 to 63 Hz, derated 10% at 50 Hz.

Constructed around an integral chassis and heat sink, with open sides, both supplies are inherently protected against short circuits and overloads by a foldback circuit. Recovery is automatic. Any output can be optionally fitted with overvoltage protection; this circuit is independent of the supply and is adjustable.

Circle 180 on Inquiry Card

Graphics Display Card Interfaces to S-100 Bus-Compatible Computers

ALT-256**2 is a high resolution 256 x 256 dot matrix graphics device which plugs directly into one slot of any S-100 bus-compatible computer, such as the Altair-IMSAI. The card contains all interface electronics, a



TV sync generator, and a 65,536 x 1-bit refresh memory, therefore requiring no CPU time to refresh the screen.

Output is a composite video signal which can be connected to any TV monitor or the video portion of a TV set. Both American and European standard versions are offered.

Announced by Matrox Electronic Systems, PO Box 56, Ahuntsic Stn, Montreal, Quebec H3L 3N5, Canada, the board requires four output and one input ports (port address is selectable onboard). Two output ports store X and Y coordinates of the addressed dot; another port turns the addressed dot on or off; and the last port is used to clear or preset the entire screen.

Multiple cards can be combined to form graphics systems with grey scale or color capability. The device also can be synchronized to an external sync generator chip for use in systems where video mixing is required. Price is $395.

Circle 181 on Inquiry Card

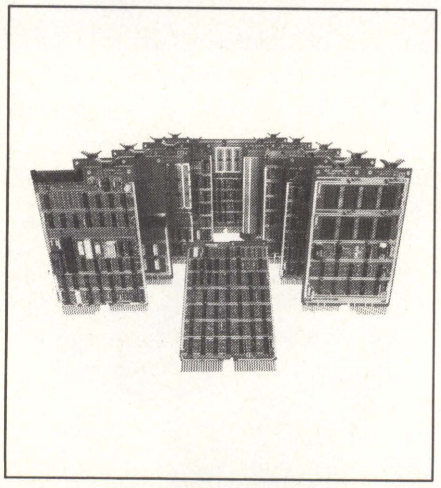
Microprogram Sequencer Is Introduced In Military Version

The 9408 microprogram sequencer, with low power Schottky compatible I/O characteristics and I^3L^{TM} technology, is available in a military temperature range version. Featuring a 10-bit program counter and 4-level subroutine nesting capabilities, it has seven test inputs. The device, from Fairchild Camera and Instrument Corp, Bipolar Memory/LSI Div, 464 Ellis St, Mountain View, CA 94042, can be operated in either a pipeline or nonpipeline mode.

Circle 182 on Inquiry Card

MDB SYSTEMS presents... The LSI-11 Connection

GP Logic Modules · Peripheral Controllers · Communications Interfaces · Special Purpose Modules · Accessory Hardware
Plus: DEC's own LSI-11 Microprocessor Module.



Here are some MDB Systems connections to LSI-11 microprocessors:

- ☐ General Purpose Interfaces:
  Parallel for programmed I/O and DMA.
  Do-it-yourself dual and quad wire wrap for any DIP design.
- ☐ Device Controllers for most major manufacturer's
  Printers
  Card equipment
  Paper tape equipment
  Plotters
- ☐ Communications/Terminal Modules
  Asynchronous Serial Line
  Synchronous Serial Line
- ☐ MDB Backplane/Card Guide Assembly (8 Quad slots)
  Rack mount chassis 5¼" front panel.
- ☐ Special Purpose Modules and Accessories
  System monitoring unit provides front panel switch addressing, power on/off sequencing; line frequency clock.
- ☐ Bus extenders/terminators.
  E-PROM and PROM modules.
  Bus connectors for backplane assemblies.

MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

MDB also supplies interface modules for DEC PDP*-11 Data General NOVA* and Interdata minicomputers.

MDB
MDB SYSTEMS, INC.
1995 N. Batavia St., Orange, California 92665
714/998-6900 TWX: 910-593-1339

*TMs Digital Equipment Corp. & Data General Corp.

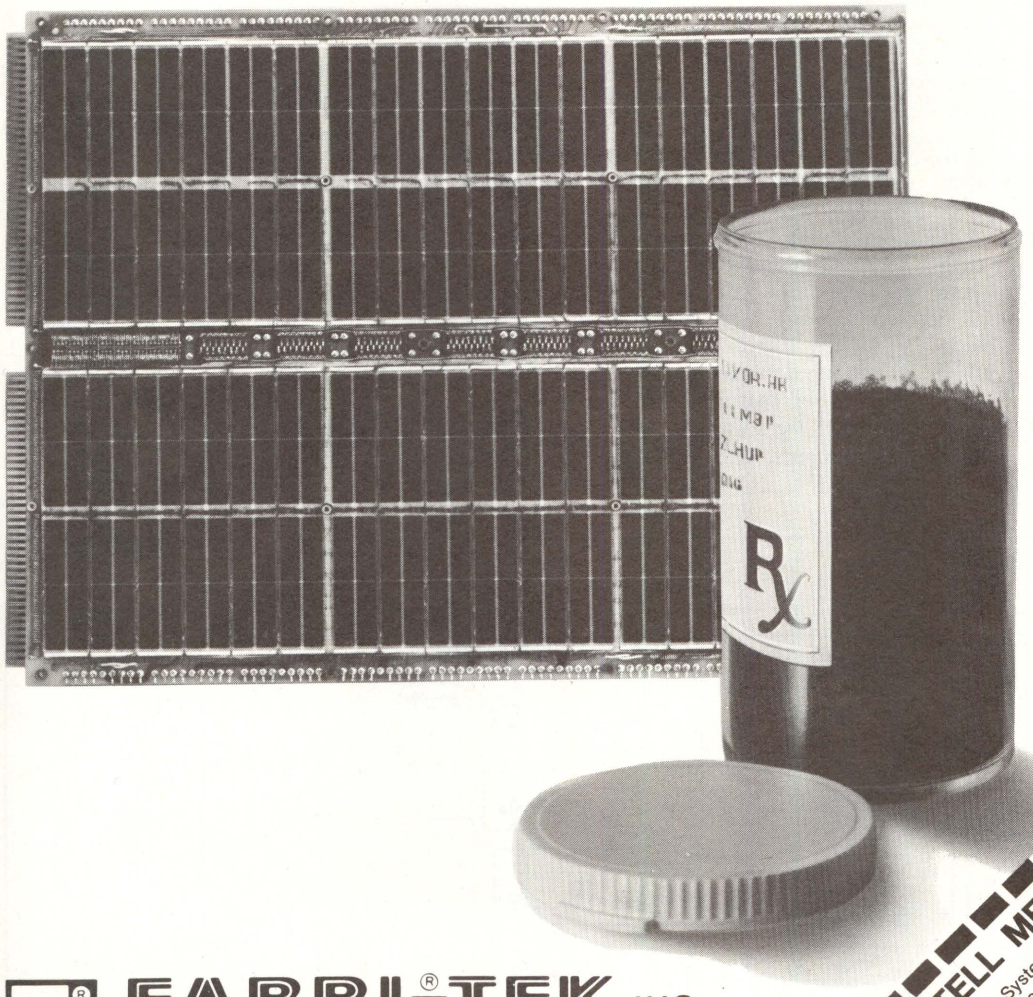
CIRCLE NO. 59 FOR LSI-11; 60 FOR PDP-11; 61 FOR NOVA; 62 FOR INTERDATA

Suffering from temporary loss of memory?

Try the Fabri-Tek core remedy.

If you're like some people who've been on a straight semiconductor memory diet, you've probably been experiencing severe complications. Loss of memory when power is removed. "Soft" random errors that can't be diagnosed. Temperature sensitivity. Added cost and complexity of error detection and correction schemes and battery back up.

For no added cost, core memories provide greater reliability, maintainability, non-volatility and 20 years of proven technology. They're relied upon in process control and a lot of other demanding applications where a failure could be catastrophic. Take our Model 698: 64K bytes of 650 nsec cycle time and 250 nsec access time. You can build a system up to 512K bytes. (Micro 3000 compatible, too). Maybe its time you kicked the semiconductor habit. We're ready to help.



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☐ Model 698-32K X18 System ☐ Model 696-16K X18 System ☐ Future requirement
☐ Bulk Core Systems ☐ 30-90 day requirement ☐ Send literature
☐ Special memory needs ☐ Have salesman call

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CIRCLE 63 ON INQUIRY CARD

High DIP-Capacity Circuit Cards Speed uProcessor System Design

A family of four high DIP-capacity circuit boards from Vector Electronic Co, Inc, 12460 Gladstone Ave, Sylmar, CA 91342 provide a combination of board sizes, power bus and ground plane organization, and edge connector configurations that speed development of microprocessor CPU, memory, or interface systems. These cards accept all DIP sockets with 0.1" (0.25 cm) by 0.3-, 0.4-, 0.6-, and 0.9-in (0.76-, 1.02-, 1.52-, and 2.29-cm) lead spacing, and with up to 64 pins.

Two 4.5 x 6.5" (11.43 x 16.51 cm) boards, 4493 and 4494 accommodate intermixed DIPs up to a max of 42 14- or 16-pin DIPs, 24 22-pin DIPs plus six 16-pin DIPs, 16 24-pin DIPs plus six 16-pin DIPs. Models 4493-1 and 4494-1 measure 4.5 x 9.6" (11.43 x 24.38 cm). They accept up to 63 14- or 16-pin DIPs, 42 22-pin DIPs plus nine 16-pin DIPs, 24 24-pin DIPs plus nine 16-pin DIPs. 4493 and 4493-1 have 72 edge contacts (36/side) on 0.1" (0.25 cm) spacing; 4494 and 4494-1 have 44 contacts (22/side) on 0.156" spacing (0.396 cm) spacing.

Full ground plane is provided on component side and power plane is provided on wiring side. Plane configuration places power supply conductors <0.25" (0.635 cm) from any DIP lead, and aids in heat dissipation. Planes exhibit a min of 430 pf distributed capacitance for low characteristic impedance on the 6.5" (16.51 cm) card.

Design provides optional area for mounting DIPs or low profile heat sink and two regulators in TO-220 packages. Leads of one regulator position are prewired to the raw power bus, ground plane, and regulated power plane. The other regulator position is uncommitted. Boards are complete with mounting holes, one heat sink, and mounting hardware. In single unit quantities, 4493 and 4494 sell for $14.95; 4493-1 and 4494-1 sell for $16.95.

Circle 183 on Inquiry Card

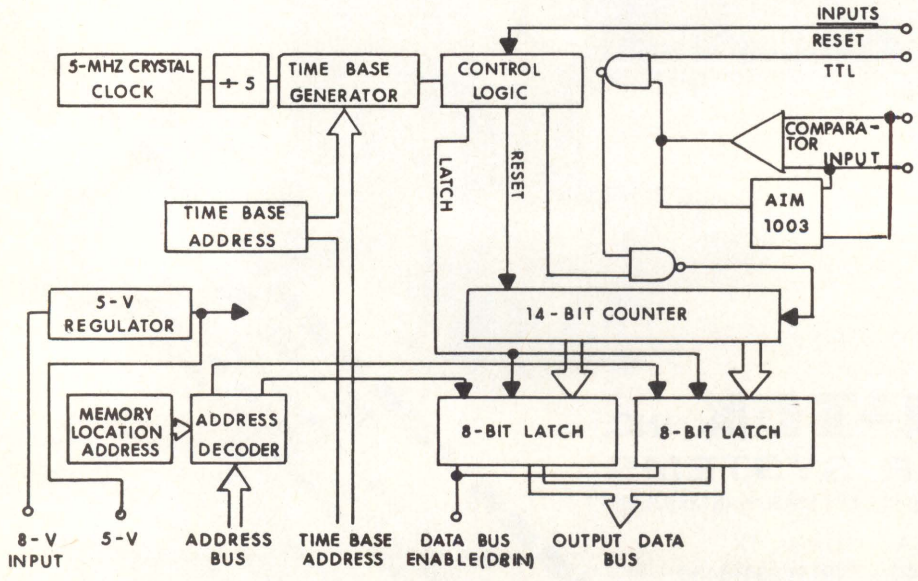
Meter Interfaces Directly With 8-Bit μComputers

The AIM-1005 frequency meter interfaces directly onto the microcomputer buses of 8-bit microcomputers and provides two 8-bit bytes of data. It has 13 bits of resolution plus overrange, and 11 time-base ranges from 10 μs to 1 hour. Interfaced as if it were memory, the device can be located in 14 different locations which are controlled with switches.

Accuracy is to within ±1 count over the 0 to 70°C operating temperature range; input frequency range is from dc to 25 MHz minimum. Input can be TTL, or the input comparator can be used, providing ±15 V of common mode and high impedance input. Optional input is an AIM-1003, which allows a transducer digitizer to be connected using a twisted pair of wires. Input connections can be made from standoffs on the top of the board, or through the edge connector.

Other features of the meter introduced by Automated Industrial Measurements, Inc, PO Box 125, Wayland, MA 01778 include compatibility with the 8080A microcomputer and an onboard 5-V regulator. Contained on a 4 x 4.5" (10.16 x 11.43-cm) PC card with 40-pin edge connector with contacts on 0.1" (0.254-cm) centers, the device is also available mounted as a daughter board on larger microcomputer cards.

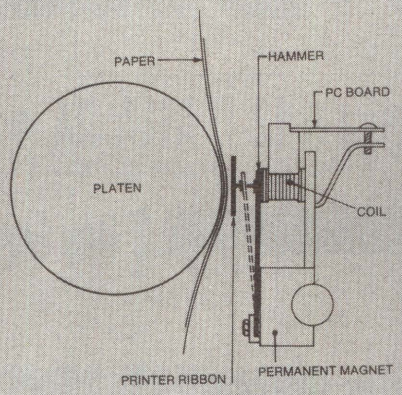
If real-time measurements are required, an external reset is provided. External reset and status flags are part of the first data byte to inform the microcomputer that a real-time measurement is taking place.



Functional block diagram illustrates Automated Industrial Measurements' 1005 frequency meter that interfaces with most 8-bit microcomputers

Circle 184 on Inquiry Card □

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

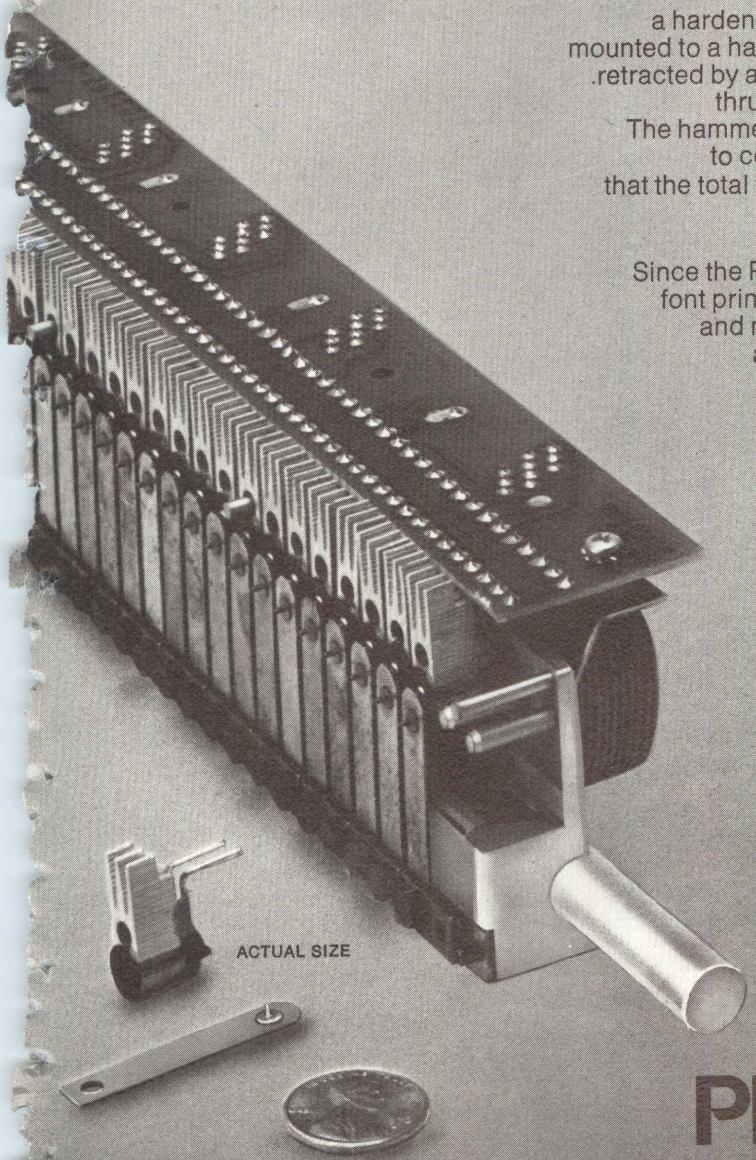


Like the far greater MTBF this elegantly simple mechanism assures.

Downtime frays nerves. It costs money, too. But take heart. You'll see a lot less of it with a Printronix 300. That's assured by its elegantly simple mechanism based on a flat strip of spring steel with a hardened tip, pictured below. Forty-four springs, or hammers, are mounted to a hammer bank. Each is fastened at one end and normally held retracted by a permanent magnet. (See the diagram.) A pulse of current thru a coil at the tip end of the hammer releases it to print a dot. The hammer bank is shuttled horizontally 0.3″, enabling each hammer to cover the space between its tip and the tip of the next one, so that the total field covered is 132 columns. Aside from paper and ribbon feed, that is the only mechanical motion in the printer.

Since the Printronix 300 has 50% fewer components than mechanical font printers . . . a head life 4 to 8 times longer than serial printers . . . and never needs adjustments of hammer flight time or character alignment as drum/chain/belt printers do, you can see why it has a longer MTBF, and why we've felt comfortable offering a one-year warranty from the beginning.

Send for our brochure. You'll discover why it produces 300 lpm print quality others can't match, has a shorter MTTR, and can give you full plotting capability . . . at no extra cost! Printronix, Inc., 17421 Derian, Irvine, CA 92714. (714) 549-8272.





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INTEGRATED COMPUTER SYSTEMS, INC.

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Microprocessor Project Management

From design through manufacture, QA and field service

MICROPROCESSORS: HOW CAN YOU GO WRONG ??? WHAT ABOUT . . . ?

Underestimating software costs and time?
Inadequate software documentation?
Selecting the wrong microprocessor?
Software development equipment($14000!)?
Manufacturing problems? Hardware/software testing? Reliability? Obsolescence? . . .

A microprocessor project is different from anything you've managed before. You can learn the right way, taught by experts, or you can struggle through the school of hard knocks (where the tuition can *really* be high!)

This unique course synthesizes the experience of hundreds of project managers (who learned the hard way) into a practical field-proven methodology for managing all phases of a microprocessor application. The course emphasizes high-risk, high-cost and time-critical problems unique to microprocessors. Concrete real-world case studies illustrate the methods presented, and these step-by-step methods can be immediately applied to your own project.

This course will benefit every manager and engineer concerned with microprocessors. Multifunctional teams from engineering, manufacturing, QA, and field service are encouraged to attend (team discounts available).

KEY TOPICS

1. **Fundamental concepts, definitions and jargon.**
2. **Avoiding pitfalls and "technical tunnel-vision."**
3. **The microprocessor application cycle: why it differs.**
4. **Planning and specifying the project — the PERT chart structure for microprocessor projects.**
5. **How to select personnel and evaluate performance.**
6. **How to select the right microprocessor — what's really important?**
7. **Software development and test equipment — what's really needed?**
8. **How to estimate overall project costs and schedule.**
9. **How to manage software design and development.**
10. **Software documentation — a practical methodology.**
11. **Verifying that the software works.**
12. **Manufacturing microprocessor-based products.**
13. **Testing and QA — software, components and products.**
14. **Component and product reliability.**
15. **Servicing microprocessor-based products.**
16. **How to prepare for the future today . . . and avoid obsolescence tomorrow.**

COURSE 102s: One Day—WEDNESDAY

Microprocessors and Microcomputers:

A Comprehensive Technical Introduction and Survey

This course provides a comprehensive unbiased introduction to microcomputer hardware/software development and integration. The course emphasizes the factors affecting key design and development decisions including: processor selection, I/O and software design, software implementation steps, development and test equipment, and most important pitfalls to be avoided when getting started. Throughout the course, applications examples provide concrete illustrations of concepts presented and are drawn from the following application areas: military, communications, consumer, instrumentation, industrial control, and biomedical systems.

This course is *vital* (1) to all engineers and managers who want a quick, unbiased, cost-effective introduction to microprocessors (2) to those engineers attending this as the first day of the "Engineering Design" series (Course 102s and 125) and (3) to managers attending this course as the second day of the "Project Management" series (Course 111 and 102s).

COURSE OUTLINE

1. **INTRODUCTION**
   • What is a microprocessor (μp)? a microcomputer (μc)? • Identifying suitable and unsuitable applications
2. **FUNDAMENTAL MICROCOMPUTER CONCEPTS**
   • Terminology • Software (SW) — how it works; how it's develope
   • Hardware (HW) — Basic μc configurations • The μc design cyc
3. **THE HARDWARE**
   • μp architectures (4, 8, 16-Bit and slices) • Memory systems design — ROM, PROM, RAM, CORE • Input/output organization (programmable I/O, interrupts, DMA) • Build or buy?
4. **INTERFACING TO THE EXTERNAL WORLD**
   • I/O port design • Programmable LSI I/O chips • Interfacing to: analog devices, keyboards, displays, cassettes, etc.
5. **SOFTWARE DESIGN & IMPLEMENTATION**
   • Four implementation methods • Editors, assemblers, compilers
   • Assembly vs. high level languages (FORTRAN, BASIC, PL/M)
6. **INTEGRATING AND TESTING THE HW AND SW**
   • What really useful tools are available? • What tools should you build yourself? • Isolating and fixing HW and SW bugs
7. **TECHNICAL SURVEY OF μP'S AND μC'S**
   • Intel, Fairchild, Motorola, National, Rockwell, Signetics, Texas Instruments, Zilog, and others including the new LSI minicomputers • Board-level μc systems — PROLOG, PCS, CONTROL LOGIC, WARNER/SWASEY, and others
   • A systematic, application-oriented approach to selecting the right microprocessor family.
8. **SELECTING DEVELOPMENT AND TEST EQUIPMENT**
   • Logic analyzers • SW simulators • Specialized μc debugging equipment • μc development systems • Peripherals to buy
9. **HOW TO GET STARTED**
   • What equipment to buy first • Pitfalls to avoid • Good information sources

R EDUCATION

6-19 | ANAHEIM, CALIF. • September 13-16

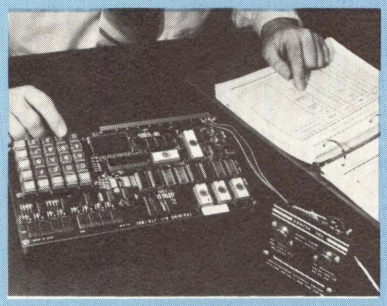
esign Series

New! Learn-By-Doing!

COURSE 125: Two Days—THURSDAY & FRIDAY

Hands-On Microcomputer Programming Workshop (for the beginner)

EACH STUDENT RECEIVES A COMPLETE 8080 MICROCOMPUTER SYSTEM FOR HIS PERSONAL USE THROUGHOUT THE COURSE.



This highly efficient, intensive short-course combines expert teachers and detailed course materials with the unique opportunity to learn by actually implementing each new programming concept *immediately* as it is developed by the instructor *on your personal microcomputer.*

COURSE OUTLINE

1. **INTRODUCTION TO THE ICS MICROCOMPUTER TRAINING SYSTEM**
   • Hardware configuration • How to use the keyboard/display and built-in commands • Exercise: Loading and executing a simple program • Exercise: Displaying results
2. **SOFTWARE FUNDAMENTALS AND BASIC TECHNIQUES**
   • The instruction cycle • CPU register instructions — Exercise: Simple arithmetic • Conditional testing and loops — Exercise: Time-delay program — Exercise: Testing individual bits • Storing/ retrieving data in memory — Exercise: Sorting a data table • Simple I/O — Exercise: Using a programmable I/O port • Subroutines — Exercise: A calculator program
3. **ADVANCED SOFTWARE TECHNIQUES**
   • Interrupt handling — Exercise: A vectored, priority-interrupt response subroutine • Real-time programming — Exercise: Organizing the I/O • Block I/O — Exercise: Real-time input of a data table • DMA I/O — Exercise: Programming a display • Multiple precision arithmetic — Exercise: 16-digit addition
4. **PROGRAM DESIGN**
   • Systems analysis • Specifying the program • Design approaches (top-down, structured programming, modular design)
5. **WHERE HIGH-ORDER LANGUAGES FIT IN**
   • BASIC • FORTRAN • PL/M • Macro's
6. **UTILIZATION OF SYSTEM DEVELOPMENT & TEST EQUIPMENT**
   • PROM programmers • Logic analyzers • Debugging tools • Full microcomputer development system with peripherals
7. **FINAL PROBLEM — IMPLEMENTING A REAL-TIME TRAFFIC CONTROLLER**
   • Specifying the problem • Partitioning the HW and SW • SW design including flow-charts • Design critique • Program implementation (using subroutines developed in class earlier) • Testing and debugging • Completing the documentation

CIRCLE 65 ON INQUIRY CARD

COURSE ENROLLMENT FORM

COURSE HOURS:

Orientation: 8:30—9:00am
Course Lecture: 9:00am—4:30pm
Microcomputer Demos: 4:30—6:00pm

In addition to the extensive hands-on exercises of Course 125, informal microcomputer hardware activities are organized at every course for valuable hands-on experience.

COURSE FEE:

Management Series: (2 days: 111+102s)—**$390**
Design Series: (3 days: 102s +125)—**$495**
Complete Series: (4 days: 111+ 102s +125)—**$595**
Individual Courses: 111—**$195**, 102s—**$195**, 125—**$395**

Course Fee Includes: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.

Team/Group Discount: 10% reduction for three or more participants from the same organization.

TO ENROLL:

Please fill out, detach and return this coupon. A confirmation with complete course details will be forwarded to you.

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ATLANTA	☐ AUGUST 16	☐ AUGUST 17	☐ AUGUST 18-19
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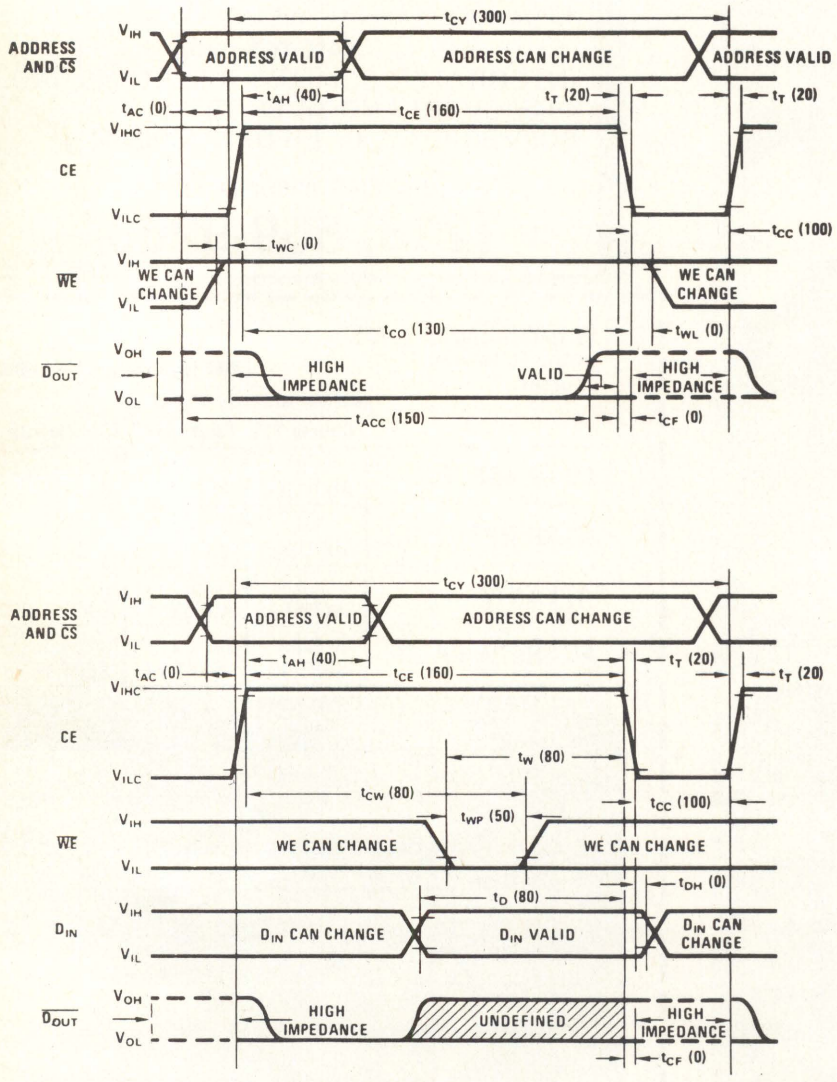
4k RAMs Feature 2 to 1 Speed/Power Improvement

"A" versions of the MM5270, MM5271, MM5280, and MM5281 4k-bit dynamic random-access memories now available from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 feature access time selections down to 10 ns, while the MM5270A and MM5280A have cycle times of 210 ns. These improved time ratings, said to be the fastest for 4k RAMs available on the market, result from use of a single-device cell that occupies only one square mil.

The devices plug into the same sockets as the older 4k RAMs; for applications where added speed is not necessary they can be run at the same speed as the older RAMs but with a 40% power saving.

Device organization is 4k x 1. Access time is 150 ns max; cycle time is 300 ns min. Address registers are on-chip and outputs are Tri-state®.

The 18-pin 5270A uses a high level chip-enable and has a Trishare® common I/O port. The 5280A uses the same clock level, but has 22 pins and a separate input and output; while the 5271A and 5281A have the TTL-compatible chip enable. The 18-pin devices require 12- and −5-V power supplies, while the 22-pin devices need an additional 5-V supply.



Switching time waveforms for National Semiconductor MM5280A: (top) read and refresh cycle; (bottom) write cycle. Series are claimed to be fastest 4k RAMs available on market

Add-In Memories For PDP-11/04 and /34 Have 64k-Word Capacities

Available with or without parity, two add-in memories fit into single hex wide slots in PDP-11/04 and /34 computers and are completely hardware and software compatible. MSC 3501 can be populated to 16k words in 4k-word increments, 3603 to 64k words in 16k-word increments. Both are available from Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110 in depopulated format for later expansion as memory requirements increase. High speed versions are claimed to provide 17% faster data throughput than the original manufacturer's memory.

Circle 350 on Inquiry Card

Add-On RAM Systems Improve Large Computer Price-Performance

A family of "universal memory systems" is claimed to dramatically improve memory performance for medium and large IBM System 370 computers while reducing the number of add-on devices needed for storage capacity expansion. Announced by Intersil, Inc, 1275 Hammerwood Ave, Sunnyvale, CA 94086, the memory systems are transferable among compatible 370 computer models with minimal interfacing changes.

The memory systems are field upgradeable to twice the storage capacity presently available from the computer manufacturer. Interchangeability provides end-users with both immediate improved price-performance and continuing cost savings

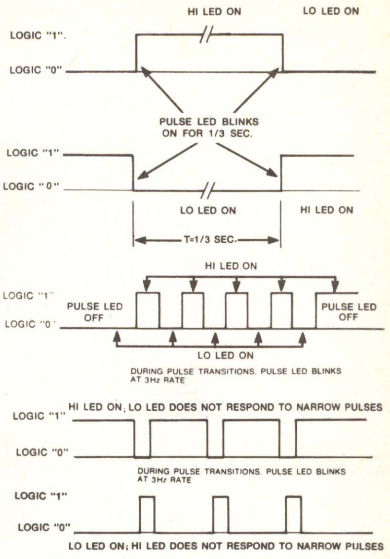
Logic Probe 1 is a compact, enormously versatile design, test and troubleshooting tool for all types of digital applications. By simply connecting the clip leads to the circuit's power supply, setting a switch to the proper logic family and touching the probe tip to the node under test, you get an instant picture of circuit conditions.

LP-1's unique circuitry—which combines the functions of level detector, pulse detector, pulse stretcher and memory—makes one-shot, low-rep-rate, narrow pulses—nearly impossible to see, even with a fast scope—easily detectable and visible. HI LED indicates logic "1", LO LED, logic "0", and all pulse transitions—positive *and* negative as narrow as 50 nanoseconds—are stretched to ⅓ second and displayed on the PULSE LED.

By setting the PULSE/MEMORY switch to MEMORY, single-shot events as well as low- rep-rate events can be stored indefinitely.

While high-frequency (5-10MHz) signals cause the "pulse" LED to blink at a 3Hz rate, there is an additional indication with unsymmetrical pulses: with duty cycles of less than 30%, the LO LED will light, while duty cycles over 70% will light the HI LED.

In all modes, high input impedance (100K) virtually eliminates loading problems, and impedance is constant for all states. LP-1 also features over-voltage and reverse-polarity protection. Housed in a rugged, high-impact plastic case with strain-relieved power cables, it's built to provide reliable day-in, day-out service for years to come.



CSC'S MULTI-FAMILY LOGIC PROBE 1. AT $44.95, IT DIGS UP A LOT OF INFORMATION WITHOUT BURYING YOUR BUDGET.

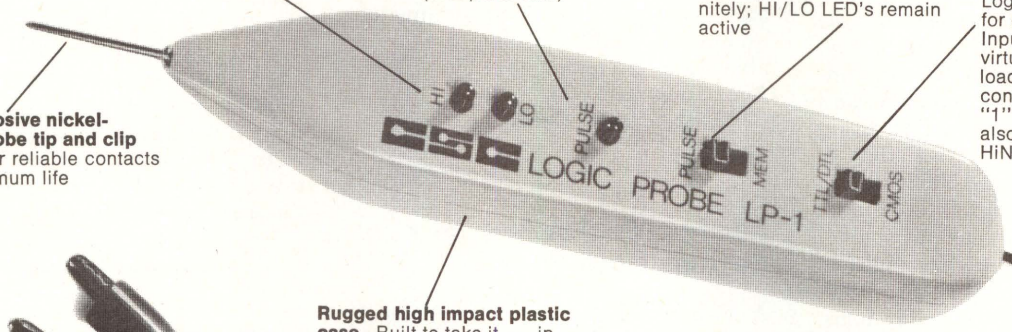
HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity at node under test

PULSE LED—Lets you know what's going on—and off. Indicates positive *and* negative pulse and level transitions. LP-1 stretches pulses as narrow as 50 nanoseconds to full ⅓ sec. (3Hz pulse rate)

PULSE/MEMORY Switch—PULSE position detects and stretches pulses as narrow as 50 nanoseconds to ⅓ sec. Switch to MEMORY and it stores single shot and low-rep-rate events indefinitely; HI/LO LED's remain active

Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels, for greater versatility. High Input Impedance—100K virtually eliminates circuit loading problems and is constant in both "0" and "1" states. CMOS position also compatible with HTL, HiNIL and MOS logic

Non-corrosive nickel-plated probe tip and clip leads—For reliable contacts and maximum life



Rugged high impact plastic case—Built to take it . . . in the lab or in the field

Protected—Features built-in reverse polarity and over-voltage protection; strain-relieved power cable

$44.95 Price tag—Costs so little it can be *your* personal property

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from simplified installation and reduced backup requirements.

UMS-1, designed for interchangeable use with System 370/158 and /168 computers, uses 8k RAMs that are claimed to be the fastest high density RAMs available for systems use today. Fully compatible with earlier 4k systems, this unit is field upgradeable to 16M bytes and will be upgraded with 16k RAMs when available next year.

UMS-2 replaces as many as four add-on memory models previously required to upgrade 370/135, /145, /138, and /148 computers. Early units will use 2k static RAMs, but later models will be field upgradeable to 4M using 4k static devices.

Circle 351 on Inquiry Card

LCD and Shift Register CMOS ICs Introduced

Three devices have been announced by Hughes Aircraft Co, MOS Products, 500 Superior Ave, Newport Beach, CA 92663 as additions to the available CMOS circuits. One is an LSI IC for converting multiplexed BCD information into signals suitable for driving a liquid crystal display. HMUX0190, a 40-pin device, is compatible with a 4-decade counter, and can be applied in any system using a parallel-drive liquid crystal display with 4-digit multiplexed BCD input, such as an LCD digital voltmeter.

The other two circuits are monolithic dual 16-bit static shift registers designed for applications in 4000-series CMOS digital logic systems. They are compatible with TTL and DTL levels and are capable of 2-MHz data rates. Each features single-phase clock and full static operation. Operating temperature range is −55 to 125°C. HSSR0321 is a 16-pin plastic or ceramic DIP while HSSR0351 is packaged in an 8-pin TO header.

Circle 361 on Inquiry Card

Programmable Circuit Handles Multi-Protocol Communications Data

Serial digital data can be formatted, received, and transmitted in all synchronous data communications protocols through use of a multi-protocol communications controller. The 2652 LSI chip supports bit-oriented protocols such as SDLC, HDLC, and ADCCP and byte-oriented protocols such as BISYNC and DDCMP at data rates up to 500k bits/s. It requires only a single 5-V power supply.

Both receiver and transmitter sections are double buffered and operate in either half- or full-duplex modes. The fully TTL-compatible chip can be interfaced with 8- or 16-bit data buses.

Interface between controller chip and communications control processor is via a 16-bit 3-state data bus and associated control signals. Corresponding high and low order bits can be wire ORed to interface with an 8-bit processor. Four internal 16-bit registers can be individually addressed as 16-bit words or 8-bit bytes.

Two of these registers contain common parameter information for application configuration. A receiver buffer register contains data and status information, while a transmitter buffer register contains data and control information.

Additional chip features include programmable SYNC or secondary address comparison, programmable CRC generation and checking, programmable character length selection, short character detection, automatic detection and generation of special control characters such as FLAG and ABORT, and automatic zero deletion and insertion. Sample or production quantities of the controller are available from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 352 on Inquiry Card

Semiconductor Memory Retains Data 96 Hours

A 4k-byte OEM memory card which retains data in standby at least 96 hours after a system power supply failure or shutdown is intended for use as either standby or main memory in mini- or microcomputer systems. The in-8100 nonvolatile RAM module, from Intel Memory Systems, 1302 N Mathilda Ave, Sunnyvale, CA 94086, contains a resident standby power supply consisting of battery charger, flat nickel-cadmium battery, and an interface that senses loss of system power and puts the memory on standby power. In normal operation, the module draws 1.7-A max current from a single 5-V power supply.

Data are stored in an array of CMOS static RAMs. The basic card operates in two jumper-selectable modes: 2k words x 16 bits or 4k words x 8 bits. A TTL-compatible bus interface provides 16 bidirectional data I/O lines, 16 address inputs, and control lines. The module expands to 65k 8-bit words or 32k 16-bit words of directly addressable storage.

Operation is fully static. Read access time is 720 ns; read and write cycle times are 770 ns.

Modules are 12 x 6.75″ (30.48 x 17.1 cm) and can be mounted on 0.6″ (1.5-cm) centers in a card cage. Ambient temperature range is 0 to 55°C for both standby and normal operation.

Circle 353 on Inquiry Card

Volume EROMs Available

Four types of ultraviolet-light erasable read-only memories—the MCM68708L, 68A708L, 2708L, and 27A08L—are now in volume production at Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721. The memories are organized as 1k x 8 bits and are pin-for-pin compatible with the MCM65308, 68308, and 2308 mask-programmable ROMs. They are said to be particularly cost-effective in those applications where small quantities of many memory patterns are required or for prototyping new systems.

68708L and 68A708L units are bus-compatible with M6800 microcomputer systems and have access times of 450 and 300 ns, respectively; 2708L is a replacement for the Intel 2708 (450-ns access time); while 27A08L is a 300-ns part for upgrading 2708 systems. All are specified for 0 to 70°C operating ambients and use 12-, 5-, and −5-V supplies.

Circle 354 on Inquiry Card

Hex Digit Driver Interfaces MOS/CMOS To High Current Loads

D140, said to be the first digit driver to operate from a supply voltage as low as 3 V, directly interfaces low voltage MOS/CMOS LSI to high current loads. The hex digit driver operates at from 3 to 6 V and features 90-mA output sinking capability with a 3-V supply, MOS-compatible inputs, <1-mA standby power, and <250-ns switching speed. Each of six independent drivers on the monolithic bipolar chip contains a high gain Darlington stage and input current limiting resistor network.

Low input voltage requirement simplifies interface to MOS LSI circuits in battery-operated systems, such as handheld instruments with

advance program

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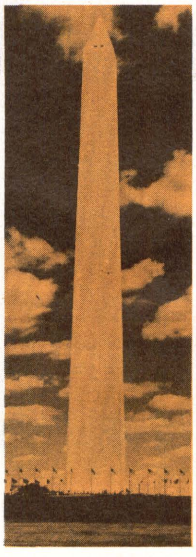


TUTORIALS Tuesday, September 6, 1977

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- The Use of Precise Specification in the Development, Testing and Control of Software
- The Design and Application of Microprocessor Systems
- Distributed Processing: the Emerging Technology

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September 6-9 **fall**

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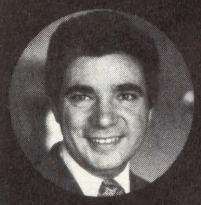
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fall COMPCON 77

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An exceptional offering for the professional programmer to upgrade his skills in a highly technical tutorial session.

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University of North Carolina

David Gries
Cornell University

The Design and Application of Microprocessor Systems

The workshop will include a variety of problem solving exercises with 'hands-on' hardware for the participants.

Roger Westgate
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Distributed Processing

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• The Use of Precise Specification in the Development of Software

COURSE OUTLINE:

The tutorial will cover the latest techniques in the use of precise specification in the development of software. Topics to be covered include:

- The division of software projects into work assignments (modules).
- The use of specification techniques to document decisions about the interfaces between the modules.
- The design of appropriately abstract interfaces.
- The use of correctness ideas in the development of correct programs from specifications.

LECTURERS:

Dr. David Parnas is a Professor of Computer Science at the University of North Carolina at Chapel Hill. His work has been in the areas of software engineering and operating systems. He received the Ph.D. degree in systems and communications sciences from Carnegie Institute of Technology in 1965.

Dr. David Gries is an Associate Professor of Computer Science at Cornell University. His work has been in the areas of programming methodology, programming languages design and compiler writing. He received the Dr. rer. nat. degree in mathematics from the Technische Hochschule Munich, Germany, in 1966.

• The Design and Application of Microprocessor Systems

COURSE OUTLINE:

The tutorial will cover a broad spectrum of microprocessor technology and applications. Topics to be covered include:

- Advanced microprocessor technology.
- Memory components and systems.
- Single chip processors.
- Interfacing to microprocessors.
- Programmable I/O chips.
- Bit-slice processors.
- Development systems.
- Software aids.

A 'hands-on' workshop will be a highlight of the microprocessor tutorial.

LECTURER:

Dr. Roger Westgate is a Professor of Electrical Engineering at Johns Hopkins University. His work has been in the areas of electronic devices, circuits and microprocessors. He received his Ph.D. degree from Princeton University in 1966.

• Distributed Processing

COURSE OUTLINE:

The tutorial will address technological and managerial considerations in the design and application of distributed processing. Three broad categories of distributed systems will be discussed:

- Placing intelligence at the point of need.
- Resource sharing networks.
- Construction of Powerful Computing Systems by coupling multiple small computers.

LECTURERS:

Burt H. Liebowitz is Vice President of International Computing Company. He has twenty years of experience in the computer field, the last five of which have been involved with distributed systems.

Dr. John Carson is a computer scientist with RLG associates, Inc., Reston, Virginia. He is currently involved in the design and implementation of specially configured multiprocessor systems.

BOTH TUTORIALS START 9:00AM, TUESDAY, SEPTEMBER 6, 1977

REGISTRATION FOR TUTORIALS AND CONFERENCES ON LAST PAGE

WEDNESDAY September 7, 1977

9:30 PLENARY SESSION

Welcome and Awards
Merlin Smith, President, IEEE Computer Society
Paul L. Hazan, COMPCON 77 FALL General Chairperson
Paul S. Skartvedt, COMPCON 77 FALL Program Chairperson

Conference Keynote Address

11:00 TECHNICAL KEYNOTE SESSIONS (Parallel)

COMPCON SPECIAL FEATURE: FORECAST OF COMPUTER TECHNOLOGY, 1977-1985
Isaac Auerbach, President, Auerback Publications

MICROPROCESSORS: MICROPROCESSORS; THEIR IMPACT ON DESIGN ENGINEERING
Eugene McFarland, Asst. V.P., MOS Division, Texas Instruments

11:30 TECHNICAL KEYNOTE SESSIONS (Parallel)

COMPUTER APPLICATIONS: APPLICATION TRENDS AND DIRECTIONS
Joe M. Henson, Vice President, Market Planning, Data Processing Division, IBM

COMPONENT TECHNOLOGY AND MEMORIES: TRENDS IN FUTURE MEMORY DEVELOPMENT
Tom Klein, National Semiconductor Corp.

12:00 TECHNICAL KEYNOTE SESSIONS (Parallel)

DISTRIBUTED PROCESSING: AN OVERVIEW OF DISTRIBUTED PROCESSING
E. Douglas Jensen, Honeywell Systems & Research Center, Minneapolis, Minnesota

PERIPHERALS: PERIPHERALS IN THE FUTURE

12:30 TECHNICAL KEYNOTE SESSIONS (Parallel)

SOFTWARE: CAN SOFTWARE BE MORE LIKE HARDWARE? SHOULD IT BE?
Walter Beam, U.S. Air Force, Office of the Assistant Secretary, Deputy for Advanced Technology

SYSTEM TECHNOLOGY: TRENDS IN COMPUTER SYSTEM TECHNOLOGY AND ARCHITECTURE
Edson De Castro, President, Data General Corp., Boston, Massachusetts

1:00 LUNCH

WEDNESDAY AFTERNOON (Parallel Sessions)

2:30 SESSION 1 (SOFTWARE)
SOFTWARE PERSONNEL DEVELOPMENT

Chairperson: D.S. Johnson, Texas Instruments
"AIR FORCE CONTINUING EDUCATION IN SOFTWARE ACQUISITION AND ENGINEERING," Capt. J.B. Peterson, AFIT, Wright Patterson AFB
"THE EDUCATION OF SOFTWARE MANAGERS IN INDUSTRY," L.K. Jensen, TRW Defense & Space Systems Group

SESSION 2 (COMPONENT TECHNOLOGY AND MEMORIES)
TOPICS IN MEMORY TECHNOLOGY

Chairperson: Joel Karp, Ram Power Inc., Palo Alto, California
"STATUS OF SEMICONDUCTOR MEMORY IN JAPAN," Toshio Kurosawa, Nippon Electric Co. Ltd., Japan
"BUBBLE MEMORY PERFORMANCE IN SYSTEM DESIGN," Paul White, Burroughs Corp., MCO, San Diego, California

SESSION 3 (DISTRIBUTED PROCESSING)
HIERARCHICAL CONFIGURATIONS

Chairperson: Grayce Booth, Honeywell Information Systems
"HIERARCHICAL CONFIGURATIONS FOR DISTRIBUTED PROCESSING," Grayce Booth, Honeywell Information Systems
"SOME REALITY TO HIERARCHICAL SYSTEMS," David Slone, GE Telecommunications & Information Systems

4:00 SESSION 4 (SYSTEM TECHNOLOGY)
ARRAY AND DIRECTED APPLICATIONS

Chairperson: Howard Johnson, System Development Corp.
"THE ARRAY 2 PROCESSOR," Paul B. Schneck, NASA
"A PIPELINED ARCHITECTURE BIT-SLICE COMPUTER FOR HIGH LEVEL LANGUAGE," Jean Pierrre Schoellkopf
"THE EVOLUTION OF PARALLEL PROCESSOR ARCHITECTU FOR IMAGE PROCESSING," John Franks, Goodyear Corp.

SESSION 5 (APPLICATIONS)
AUTOMATIC TEXTURE ANALYSIS OF MEDICAL IMAGES

Chairperson: R. Ledley, National Biomedical Foundation, Georgetown University
"TEXAC: A SPECIAL PURPOSE PICTURE PROCESSING TEXTURE ANALYSIS COMPUTER," R.S. Ledley and L.S. Rotolo, National Biomedical Foundation
"INTERACTIVE IMAGE PROCESSING SYSTEMS," C. Harlow, L. Cook, P. Cook, S. Dwyer, University of Missouri
"TEXTURE ANALYSIS IN WHITE BLOOD CELLS IMAGE PROCESSORS," K. Preston, Jr., Carnegie-Mellon University

SESSION 6 (PERIPHERALS)
ADVANCED PERIPHERALS & TECHNOLOGIES

Chairperson: J. Egil Julliusen, Texas Instruments
"NEW FREEDOMS IN COMPUTER OUTPUT PRINTING," J.L. Johnson, Magnetic Peripherals Inc., Oklahoma City, Oklahoma
"DESIGN AND SIMULATION OF A CCD BASED DISPLAY MEMORY SYSTEM FOR A MICROCOMPUTER CONTROLLED CRT TERMINAL, K.D. Geist and C.A. Papachristou, Drexel University, Philadelphia, Pennsylvania
"PORTABLE BUBBLE TERMINAL – ADDED DIMENSION TO REMOTE DATA ENTRY," S. Flannigen

WEDNESDAY EVENING

5:30 COMPCON Cocktail Party

7.00 DOD STANDARDIZATION PANEL

THURSDAY September 8, 1977

THURSDAY MORNING (Parallel Sessions)

9:00 SESSION 7 (SOFTWARE)
SOFTWARE MANAGEMENT DISCIPLINE

Chairperson: Lt. Col. Alan Salisbury, U.S. Army ARTADS, Ft. Monmouth, New Jersey
"THE MANAGER AS AN ABSTRACT SYSTEM," M.H. Hamilton Higher Order Software, Inc.
"SOFTWARE MANAGEMENT DISCIPLINE: A COMMERCIAL VENDOR VIEWPOINT," W.C. Cave, U.S. Army ARTADS/CENTACS, Ft. Monmouth, New Jersey
"A PROJECT MANAGEMENT SYSTEM FOR SOFTWARE DEVELOPMENT," R.W. Spitler, Merrill Lynch, New York

SESSION 8 (PERIPHERALS)
STATE OF THE ART STORAGE TECHNOLOGY AND DEVICE

Chairperson: L. J. Mathews, Magnetic Peripherals, Inc.
"THIN FILM TECHNOLOGY FOR HEADS AND DISKS"
"MOVING HEAD, FIXED AND REMOVABLE MEDIA, DISK STORAGE TRENDS"
"NEW MASS STORAGE APPROACHES AND IMPACT ON A CURRENT DISK DRIVE"

SESSION 9 (SYSTEM TECHNOLOGY)
IMPLEMENTATION TECHNIQUES FOR NEXT GENERATION SYSTEMS

Chairperson: J.R. Leonardi
"DBS ARCHITECTURE AND THE FUNCTIONS IT SHOULD SUPPORT," D.Z. Badal, University of California, Los Ange
"DESIGN TOOLS FOR MICROPROGRAMMABLE MICROPROCESSORS," K.R. Dimond/J.A. King, University of Canterbury at Kent
"MULTIMICROPROCESSOR ARCHITECTURES AND THE USE OF MULTILEVEL ENCODING IN MICROINSTRUCTION FORMATS," C.V.W. Armstrong

11:00 SESSION 10 (MICROPROCESSORS)
HIGH LEVEL LANGUAGES FOR MICROS

Chairperson: Terry Dolhoff, Acuity Systems
"SYSTEMS LANGUAGES, WHERE DO THEY FIT?"
"BASIC: THE HOBBY STANDARD"
"ASSEMBLY LANGUAGE – FOR BETTER OR FOR WORSE," Terry Dolhoff, Acuity Systems

SESSION 11 (DISTRIBUTED PROCESSING)
MODELS AND SIMULATION FOR DISTRIBUTED PROCESSING

Chairperson: Stephen R. Kimbleton, NBS
"RESULTS OF A GPSS SIMULATION OF THE AFOS CLOSED LOOP STORE-AND-FORWARD COMMUNICATIONS NETWORK," M.S. Goldman and Dr. S.N. Wei, National Weather Service, Silver Spring, Maryland
"DESCRIPTION AND REALIZATION OF PARALLEL CONTROL SYSTEMS," M. Courvoisier, Centre National De La Recherche Scientifique, France
"JOB ALLOCATION IN A DISTRIBUTED COMPUTER NETWORK," Glenn R. Linsenmayer and P. Ligomenidis, Glen Burnie, Maryland

SESSION 12 (SOFTWARE)
SOFTWARE ENGINEERING AND DEVELOPMENT FOR MICROPROCESSORS

Chairperson: Barry Press, TRW Defense & Space Systems Group
"MICROPROCESSOR SOFTWARE ENGINEERING," Col. F.J. Hilbing, Rome Air Development Center, USAF
"A HIGH LEVEL MICROPROCESSOR PROGRAMMING LANGUAGE," D.F. Furgerson and A.J. Gibbons, Westinghouse Electric Corp.
"USING HIGH LEVEL LANGUAGES TO PRODUCE LOAD MODULES FOR ROM IN MEDIUM (2000) QUANTITIES," L. Saunders, Tetronix, Inc.

1:00 LUNCH

THURSDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 13 (MICROPROCESSORS)
MICROCOMPUTER DEVELOPMENT TECHNIQUES

Chairperson: Theodore Powell, Texas Instruments
"HELP FOR MICROPROCESSOR SOFTWARE DEVELOPMENT," H.A. Cohen and R.S. Francis, Latrobe University, Australia
"INTEGRATING MICROCOMPUTERS HARDWARE AND SOFTWARE DEVELOPMENT TOOLS," Marvin Conrad, Texas Instruments
"UNIVERSAL MICROPROCESSOR SYSTEMS SOFTWARE," W.H. Burkhardt, Universitaet Stuttgart, Hzenbergstr

SESSION 14 (SYSTEM TECHNOLOGY)
MINI AND MULTI PROCESSORS

Chairperson: Bill Poduska, Prime Corp.
"TRENDS IN SUPERMINI ARCHITECTURE," B. Tannenbaum, & S. Wallach, Data General Corp.
"IBM SERIES ONE – AN ARCHITECTURE OVERVIEW," Stu Elder, IBM
"THE MULTIPROCESSOR SYSTEMS SMS 201," R. Kobert

SESSION 15 (COMPONENT TECHNOLOGY AND MEMORIES)
DIRECTIONS OF LOGIC TECHNOLOGY

Chairperson: L.M. Terman, IBM
Dick Pashley, INTEL Corp.
Tom Longo, Fairchild Corp.
W.V. Lin, AMDAHL Corp.

4:00 SESSION 16 (APPLICATIONS)
MILITARY APPLICATIONS

Chairperson: J.M. Wilcox, Computer Sciences Corp., Virginia
"APPLICATIONS OF MICROPROGRAMMABLE COMPUTERS FOR MILITARY SYSTEMS"
"APPLICATION OF EMULATION FOR MILITARY SYSTEMS VALIDATION, VERIFICATION AND INTEROPERABILITY TESTING"
"EMERGING SOFTWARE DEVELOPMENT METHODOLOGIES FOR MILITARY SYSTEMS DEVELOPMENT

SESSION 17 (APPLICATIONS)
DIGITAL SIGNAL PROCESSING

Chairperson: R.L. Carberry, IBM
"DEVELOPMENTS IN SIGNAL PROCESSING ALGORITHMS," T. Kriz, IBM
"SIGNAL PROCESSING ARCHITECTURAL CONSIDERATIONS," P. Kogge, IBM
"TECHNOLOGY REQUIREMENTS FOR SIGNAL PROCESSING," J. Phillips, TRW

SESSION 18 (SOFTWARE)
MODERN PROGRAMMING PRACTICES

Chairperson: R.W. Weber, ISIM Rome Air Development Center
"EFFECTS OF MODERN PROGRAMMING PRACTICES ON SOFTWARE DEVELOPMENT COSTS," R.K.E. Black, Boeing Computer Services
"IMPACT OF MODERN PROGRAMMING PRACTICES ON SYSTEM DEVELOPMENT," J.R. Brown, TRW Defense and Space Systems Group
"AN EVALUATION OF THE EFFECTIVENESS OF SOFTWARE ENGINEERING TECHNIQUES," P.C. Belford, Computer Sciences Corp.

THURSDAY EVENING

5:30 COMPCON Cocktail Party

THURSDAY EVENING PARALLEL SESSIONS

7:00 SESSION 19 (SOFTWARE)
THE NATIONAL SOFTWARE WORKS: DEVELOPMENT OF OPERATIONAL ISSUES

Chairperson: R.A. Robinson, Information Sciences Division, Rome Air Development Center
"NATIONAL SOFTWARE WORKS – OVERVIEW & STATUS," R.A. Robinson, Information Sciences Division, Rome Air Development Center
"SOFTWARE CONFIGURATION MANAGEMENT USING OPERATING SYSTEM PRIMITIVES OF THE NATIONAL SOFTWARE WORKS," N.L. Rasmussen, Gagliari Systems Group, Inc.
"SOFTWARE DEVELOPMENT FOR MINICOMPUTERS USING NATIONAL SOFTWARE WORKS TOOLS," S.L. Fleischman, Gagliari Systems Group, Inc.
"THE NATIONAL SOFTWARE WORKS: A USER APPRAISAL," N.W. Peterson, TRW Defense & Space Systems Group

SESSION 20 (SPECIAL EVENING FEATURE)
PERSONAL COMPUTING – A 'HANDS ON' SESSION AND WORKSHOP

FRIDAY September 9, 1977

FRIDAY MORNING (Parallel Sessions)

9:00 PATENT PROTECTION FOR COMPUTER PROGRAMS

SESSION 21 (COMPONENT TECHNOLOGY AND MEMORIES)
MEMORY SYSTEMS

Chairperson: Bob Welch, National Semiconductor Corp.
"STATIC OR DYNAMIC, WHICH TO USE FOR MY MEMORY SYSTEM?" J.C. Blackie, National Semiconductor Corp.
"PSEUDO RANDOM ACCESS MEMORY SYSTEM WITH CCD-SR AND MOS RAM ON A CHIP," Naoya Ohno and Katsuya Hakozaki, Nippon Electric, Japan
"ADVANTAGES OF CCD SYSTEMS IN FUTURE MACHINE ARCHITECTURE," Joe Miller, INTEL Corp.

SESSION 22 (PERIPHERALS)
SMART PERIPHERALS

Chairperson: J.S. Toreson, Microcomputer Systems Corp.
"STANDARD INTERFACES FOR MINICOMPUTERS," Gary Robinson, Inforex
"INTELLIGENT DISK, THE NEXT GENERATION," Mark Fuller, Wangco
"TERMINALS AND DATA ENTRY," Steve Star, Hewlett Packard

preliminary program continued

9:30 SESSION 23 (DISTRIBUTED PROCESSING)
NETWORKS FOR DISTRIBUTED PROCESSING

Chairperson: Stuart Wecker, Digital Equipment Corp.
"INDUSTRIAL CONTROL USING MICROPROCESSORS – THE KENT DISTRIBUTED CONTROL PROJECT," F.K. Hanna, The University of Kent at Canterbury, U.K.
"ACKNOWLEDGE ETHERNET," Mario Tokuru and Kiichiro Tamaru, Keio University, Yokohama, Japan
"A NETWORK COMPUTER FOR DISTRIBUTED PROCESSING," W. Huen, Illinois Institute of Technology

10:00 SESSION 24 (SOFTWARE)
SOFTWARE RELIABILITY ANALYSIS

Chairperson: Martin Shooman, Polytechnic Institute of New York
"A QUANTITATIVE CONNECTION BETWEEN COMPUTER PROGRAMS AND TECHNICAL PROSE," M. Halstead, Purdue University, Lafayette, Indiana
"MEASURING PROGRAM COMPLEXITY," J. Zolnowski, Texas A&M University, College Station, Texas
"STATISTICAL THEORY OF COMPUTER PROGRAM'S INFORMATION CONTENT AND COMPLEXITY," A. Laenmel, Polytechnic Institute of New York
"A GENERAL SOLUTION TO THE SOFTWARE SIZING AND ESTIMATING PROBLEM," Col. L. Putnam, U.S. Army Computer Systems Command, Ft. Belvoir, Virginia

SESSION 25 (MICROPROCESSORS)
MICROPROCESSOR BASED CONTROLLERS

Chairperson: Van Lewing, Fairchild Semiconductor
"CONTROL OF SYNCHRONOUS COMMUNICATIONS USING MICROCOMPUTER LSI PERIPHERALS," J.W. Thomas, Texas Instruments
"A MICROPROCESSOR DESIGN FOR VEHICLE CONTROL," Neal Laurance, Ford Motor Company
"A BIT SLICE MODULE SET FOR MICROCOMPUTING," Richard J. Smith, RCA

10:30 SESSION 26 (APPLICATIONS)
REAL-TIME APPLICATIONS

Chairperson: Robert New, Singer-Link Division
"EMULATION CONSIDERATIONS FOR REAL-TIME COMPUTER SYSTEMS," K.J. Thurber and G.R. Kregness, Sperry Univac, St. Paul, Minnesota
"THE SPACE SHUTTLE GROUND CONTROL SYSTEM/A NEW REAL-TIME CHALLENGE," G.H. Evans, IBM, Houston
"REAL-TIME REDUNDANCY MANAGEMENT FOR DIGITAL FLY-BY-WIRE AIRCRAFT CONTROL," E.A. Megna, MIT, and K.J. Szelay, NASA

LUNCH (12:30 and 1:00)

FRIDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 26 (COMPONENT TECHNOLOGY AND MEMORIES)
USAGE OF MEMORY COMPONENTS

Chairperson: Tom Dalfi, Intersil, Sunnyvale, California
"CCD APPLICATION," Kurt McKinsey, INTEL Corp.
"4K CMOS STATIC RAM," Shep Hume, Intersil Corp.
"ELECTRONIC MEMORY HIERARCHY," Dick Bravo, Intersil Corp.

SESSION 27 (SOFTWARE)
SOFTWARE ENGINEERING & DEVELOPMENT FOR DISTRIBUTED PROCESSING SYSTEMS

Chairperson: Clarence Giese, Ballistic Missile Defense Systems Command, Huntsville, Alabama
"SOFTWARE FOR DISTRIBUTED MICROCOMPUTER SYSTEMS," C. Whitbey-Stevens, University of Warwick, England
"THE NEED AND THE TECHNIQUE FOR IMPROVEMENTS IN REAL-TIME DISTRIBUTED CONTROL SOFTWARE," T.O. Wolff, Sperry Univac, St. Paul, Minnesota
"DERIVATION AND EVALUATION OF DISTRIBUTED COMPUTER ELEMENTS USING A DIGITAL DESIGN LANGUAGE," R.D. Ippolito, Carnegie-Mellon University, Pittsburgh, Pennsylvania

SESSION 28 (MICROPROCESSORS)
SYSTEM ENGINEERING WITH MICROS

Chairperson: Herb Arkin, Singer-Kearfott
"MULTI PROCESSOR WITH QUEUE MEMORIES," Donald R. Mott and A. Schmitz, General Electric Co.
"PROMOS – A DISTRIBUTED MICROPROCESSORS SYSTEM," Joseph C. Lombardi, U.S. Steel
"MICROPROCESSOR AVIONICS APPLICATION," N.C. Joehlin, Singer Kearfott

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LED displays, by eliminating multiple transistor arrays with associated current limiting resistors. Even at the lowest input voltage, each of the six outputs can sink high currents, desirable when driving LED common cathode digits, lamps, solenoids, or relays since it eliminates the need for costly buffering. A high impedance input eliminates the need for buffer circuitry or Darlington connections to interface inputs to the outputs of MOS/CMOS LSI circuits. Input current requirement is 150 μA max with a 3-V supply, lower than the output current capability of most LSI devices.

The device is available from Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054 in a 16-pin plastic DIP. Op temp range is 0 to 70°C.

Circle 355 on Inquiry Card

Frequency Synthesizer Suited for Multichannel Communications Use

MN6040, a single-chip phase-locked loop device, consists of a reference signal counter, programmable preset counter for frequency dividing, and phase detector. An entire PLL frequency synthesizer can be formed by adding input power, crystal oscillator, and a minimum number of other external components. The device is fabricated by the silicon-gate CMOS process using ion implantation technology and is particularly suited for use in multichannel transceivers.

Features include 10.24-MHz oscillation frequency, pure binary code used as the preset counter input, 2.55-MHz max programmable counter operating frequency, open phase detector output during lock, and protection against static charge for all preset inputs. The device is available from Energy Electronic Products Corp, 6060 Manchester Ave, Los Angeles, CA 90045.

Circle 356 on Inquiry Card

MOS ROM Generates Full ASCII Character Set

TMS4710, organized as a 1k-word x 8-bit read-only memory, outputs information for a complete set of upper and lower case ASCII characters. This includes full alphabet, periods, equal and dollar signs, 0 to 9, and other characters which have automatic spacing. Character size is 5 x 7 in 8 x 8 block format.

The device is fabricated using n-channel silicon-gate technology for high speed and simple interface with bipolar circuits. All inputs can be driven by series 74 TTL circuits with the use of external pull-up resistors, and each output can drive one series 74 TTL circuit without external resistors. Data outputs are 3-state for OR-tying multiple devices on a common bus. Two output-enable controls, when active low, allow data to be read.

Announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222, the device is designed for ASCII graphics applications such as CRT and printers. It is supplied in 24-pin DIL ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hold rows on 600-mil centers. The device is characterized for operation from 0 to 70°C.

Features include fully static operation, TTL-compatible inputs and outputs, 450-ns max access time, 450-ns min cycle time, and 310-mW typ power dissipation. Other features are two output-enable inputs for simplified system design and 8-bit output for use in microprocessor based systems.

Circle 357 on Inquiry Card

Monolithic Multiplying DAC Suited To Portable/ Military Applications

A series of 2-digit BCD monolithic multiplying digital-to-analog converters introduced by Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050 feature 85-ns settling time, complementary high compliance current outputs, universal logic inputs, and low cost. Matching between full scale and reference currents to within 1 LSB eliminates calibration in most applications. Monotonic multiplying performance is attained over a 40 to 1 reference input current range. Direct interfacing with CMOS, TTL, DTL, ECL, and HTL is provided by an optional logic threshold adjustment, and 10-μA logic inputs accept a swing of −10 to 18 V. The DAC-20 is claimed to be the first BCD DAC to interface directly with the high impedance n-MOS and p-MOS outputs of microprocessor RAMs.

It behaves as a true digitally-controlled current source; using the non-inverted or "true" output results in positive-true BCD coding, while using the complementary output results in negative-true BCD coding. Both outputs may be used simultaneously. Resistive output termination eliminates output operational amplifiers in many applications. Reference inputs accept a positive or negative dc reference, a fast pulse input, or an ac multiplying signal to beyond a 1-MHz bandwidth.

Versions are available in −55 to 125 and 0 to 70°C temperature ranges and with ±¼ or ±½ LSB nonlinearity over full temperature ranges. All models have guaranteed performance over the ±4.5- to ±18-V power supply range, with 37-mW power consumption attainable at ±5-V supplies.

Design achieves 85-ns settling times with power consumption of 37 mW at ±5 V. Full scale current drift is ±10 ppm/°C.

Circle 358 on Inquiry Card

Video Amplifiers Second-Sourced

Exact replacements for Signetics predecessors of the same designations, NE592/SE592 wideband video amplifiers are being second-sourced by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. Features include 90-MHz bandwidth, adjustable gain from 0 to 400 V/V, and adjustable bandpass to permit usage for a wide range of applications. Devices are available in combinations of 0 to 70 and −55 to 125°C, plastic or ceramic DIP, and metal can.

Circle 359 on Inquiry Card

QPL Approval Received On Schottky Devices

MIL-M-38510, Part II QPL status has been received by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040 on four low power Schottky devices for both B and C JAN levels. Government designations JM38510/30201, /30202, /30203, and /31001 (both BCB and CCB) are equivalent to industry designations 54LS40J, 37J, 38J and 11J, respectively. □

Circle 360 on Inquiry Card

PRODUCT FEATURE



Printer/Plotter is Price-Compatible With Microprocessor Systems

As low cost microprocessor-based systems continue to proliferate and to exhibit burgeoning capabilities, parallel requirements are developing for high performance peripheral devices which can be available at compatible prices. One such device is a printer/plotter introduced by Axiom Corp that is specifically designed for OEM applications requiring graphic and/or alphanumeric hard copy. The EX-810 attains an attractive cost/performance ratio through relatively simple mechanical and electronic designs and through being controlled by the user's software.

Part of the low cost/high performance goal is attained through use of a simple, high speed electrostatic printing process. Unlike impact printers which are usually limited to 12 char/in, electrostatic printout remains legible down to 20 char/in, which allows an 80-char column to be compressed from 8.5″ (21.6 cm) to 5″ (12.7 cm) without loss of readability.

Operating Principles

In the electrostatic printing process, an image is formed when current passes between an electrode and the conducting aluminum surface of the paper long enough for a small electrical arc to vaporize the aluminum directly below the electrode, exposing the colored pigment of the paper. Effectively, this image is archival.

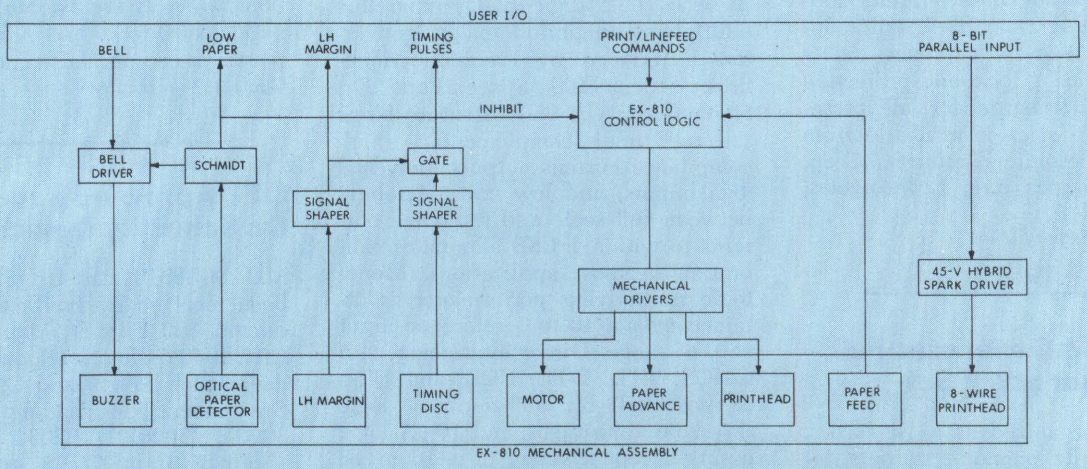
Dot matrix characters in the EX-810 are formed by selectively supplying current pulses through eight fine wires in the printhead. These wires are in light contact with the paper as the printhead moves across. A simple TTL-compatible controller enables direct control of printhead motion as well as the matrix pattern of the printout.

This controller contains the simple logic and drivers necessary to control paper feed and print solenoids as well as the 117-Vac motor. It also contains an 8-channel hybrid spark driver which converts a low power TTL input to supply the printhead with high current pulses at the 45-V level necessary to burn through the electrosensitive paper coating. Margin and position marker signals allow the input raster to be accurately synchronized with the motion of the printhead.

Plotting is achieved by outputting a parallel 8-bit pattern, synchronized to the motion of the 8-wire printhead. This allows eight rows of dots to be printed at a single pass of the printhead.

The print cycle is initiated by turning on the drive motor which also energizes feed and print solenoids. (See operational flowchart and functional block diagram.) These four solenoids pull a horizontal bar against a cam in a helical drive shaft, moving the printhead across the paper. The same movement forces the printhead against the paper under light spring action. Since the printhead assembly is only loosely coupled to the print carriage, it can adjust itself to compensate for any minor printing electrode misalignment.

Approximately 0.5 s is required to print a line or to perform a linefeed regardless of the content of the line. Thus, if a user either activated

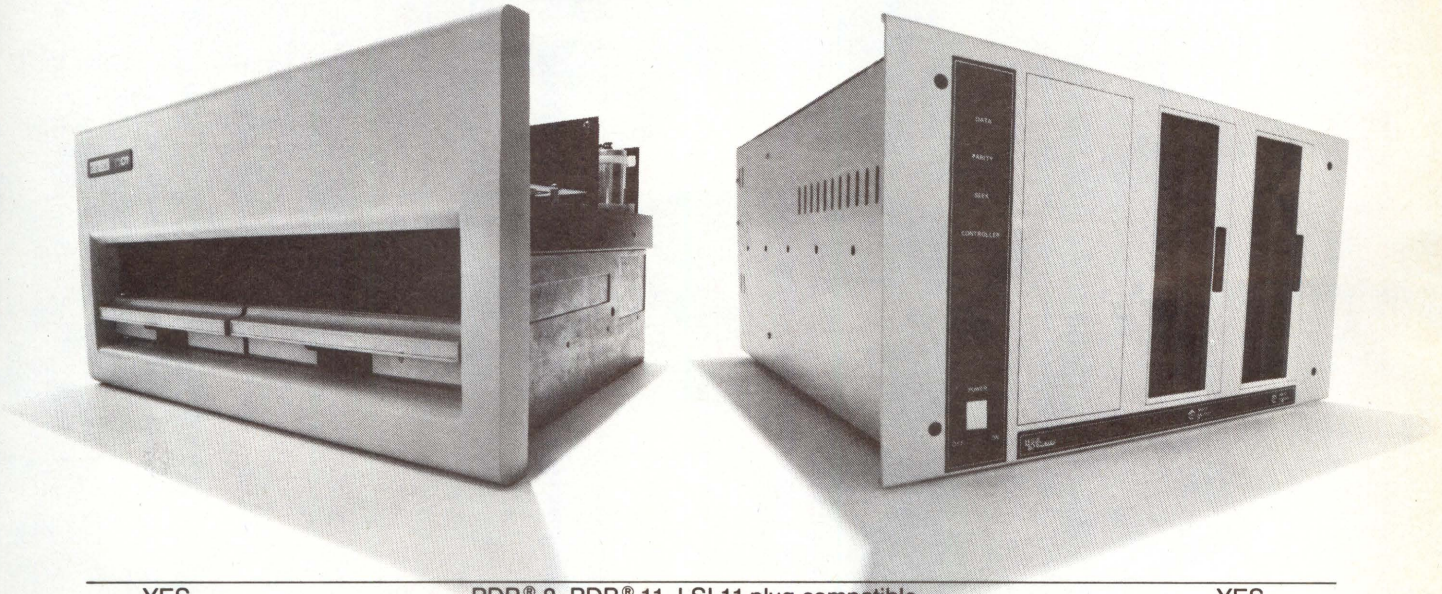


Printer/plotter functional block diagram. Printhead interfaces to user's output port through 8-channel hybrid spark driver which supplies 45-V pulses required to mark electrosensitive paper

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YES	Holds 256,256 bytes per diskette	YES
NO	Diskette formatting capability	**YES**
1 OR 2	Drives per controller	**1, 2, OR 3**
NO	Interchangeable 50/60 Hz operation	**YES**
YES	Digital phase-lock-loop data separation circuit	YES
NO	Front panel activity LED lights	**YES**
NO	Front panel system status indicators	**YES**
PARTIAL	Modular construction	**COMPLETE**
MINIMAL	Self-testing microcode	**EXTENSIVE**
NO	Field-proven Shugart drives	**YES**

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Data Systems

For an expanded comparison and complete technical details, phone or write Data Systems Design, Inc., 3130 Coronado Drive, Santa Clara, CA 95051, 408/249-9353.

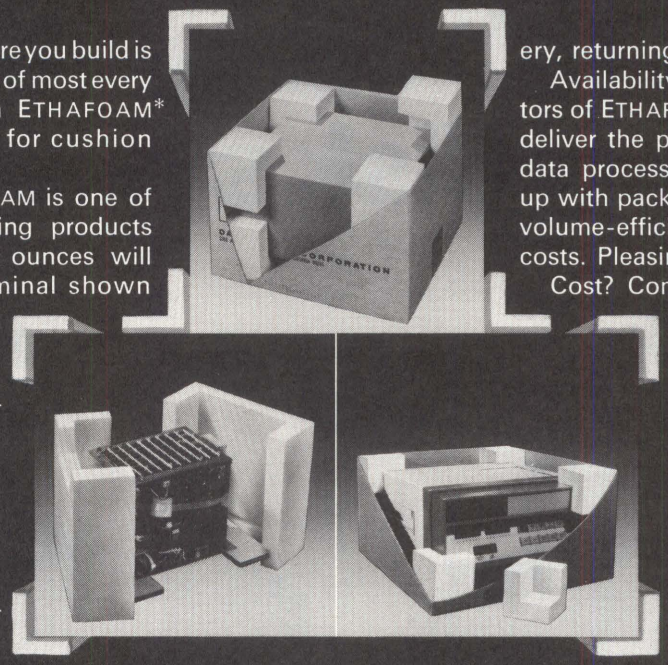
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CIRCLE 67 ON INQUIRY CARD

Why cushion packaging for data processing hardware? Because only a couple lbs. keeps more than 200 lbs. in its place.

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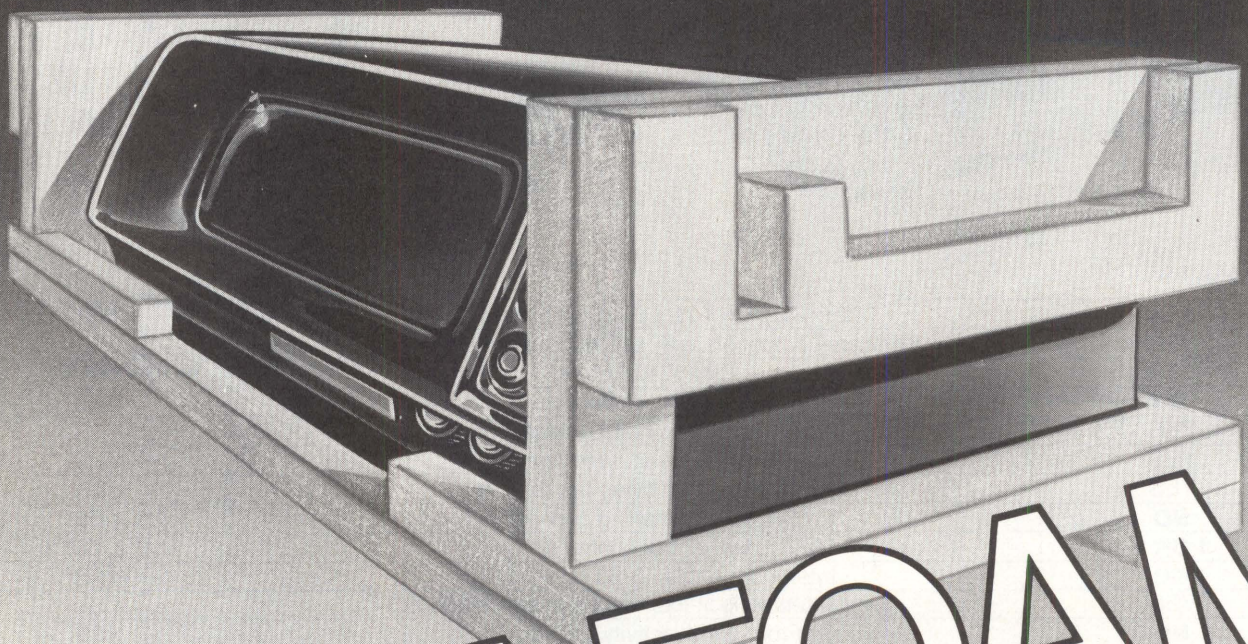
Pure and simple, ETHAFOAM is one of the most efficient packaging products you can use. Only a few ounces will protect the computer terminal shown here from impact shock, vibration and abrasion. You often get better protection than corrugated inserts provide because ETHAFOAM is a resilient closed-cell plastic foam. Often better protection than molded foam parts, too, because ETHAFOAM won't shatter and boasts excellent recovery, returning to shape after impact.



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Oakland, Tharco Precision (415) 562-9338
Santa Fe Springs, Republic Packaging (213) 921-0621
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Denver, Tharco Containers (303) 373-1860

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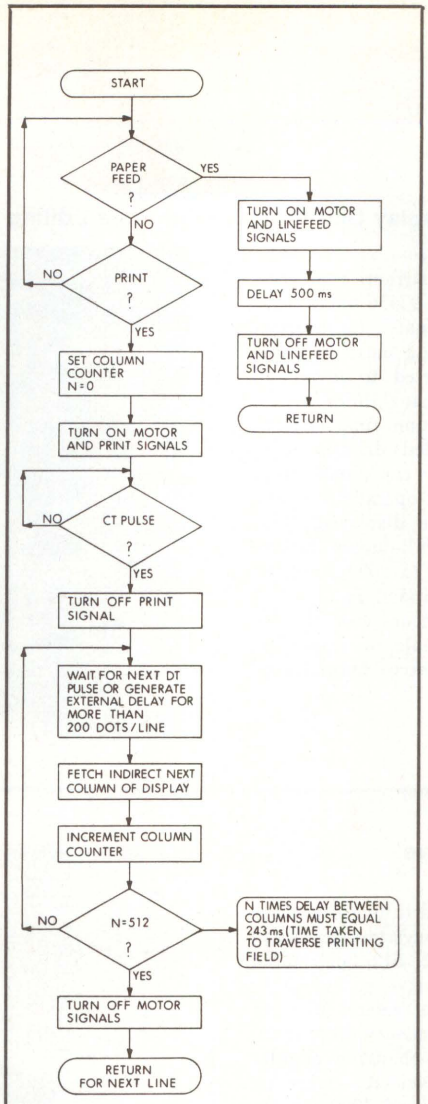
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CIRCLE 68 ON INQUIRY CARD



EX-810 operational flowchart. Character timing (CT) pulse is used as marker at beginning of each new line. Dot timing (DT) pulse as well as CT pulse give user information on exact position of printhead during plotting cycle

two line feeds or printed out 160 alphanumeric characters (using a 5 x 8 dot matrix and 80 char/line), the plotter would convert either operation into the appropriate hard copy in 1 s. Plotting is initiated by simultaneously activating motor on and print commands.

A left-hand margin signal occurs approximately 60 to 120 ms after a print cycle has been initiated. Once this signal has been given, the printhead speed is constant to within 0.1% for the entire length of time that the printhead is in the printing field.

A timing disc with two concentric sets of perforations around its perimeter acts as an optical chopper between two infrared LED photodetector assemblies. Dot timing (DT) and character timing (CT) pulses, gated by the left-hand margin signal, provide data on the exact position of the printhead during a plotting cycle. DT pulses are generated at 65/in (25.6/cm) of printhead travel; CT pulses are provided at 10/in (3.9/cm)

Vertical resolution is a function of the spacing between adjacent wires in the printhead and is fixed at 65 dots/in (25.6/cm). Horizontal internal timing resolution is the same; however, since the printhead travels at a constant speed while it is in the printing field, the user may externally generate the timing of the input bit raster to give densities of greater than 128 dots/in (50.4/cm).

Time required for the printhead to travel 4.25 in (10.8 cm) from the left-hand margin to the right-hand margin is 243 ms (0.175 in/ms or 0.444 cm/ms). Since speed of the printhead is uniform to 0.1%, if a horizontal resolution of 512 dots were required, the user could expect that the alignment of the last dot on the line would be to within one-half dot width.

Specifications

Plotting speed is two 8-row lines/s. Input raster is 8-bit parallel (active low). Paper used is 5″ (12.7 cm) wide in a standard 240-ft (73-m) roll. Thickness is 0.0024″ ±0.0004″ (61 μm ±10 μm).

Physical dimensions are 9.625 x 10.875 x 3.875″ (24.4 x 27.6 x 9.8 cm) including paper roll and top cover. Weight is 12 lb (5.4 kg).

Electrical requirements are 105 to 125 Vac, 50/60 Hz. Max power is 60 VA. Forced air cooling is required. Operating temperature is 30 to 105°F (0 to 40°C), 5 to 95% relative humidity, noncondensing.

Price and Delivery

Single unit price for the EX-810 printer/plotter is $795. OEM discounts are available. Delivery is four to six weeks ARO. Axiom Corp, 5932 San Fernando Rd, Glendale, CA 91202. Tel: (213) 245-9244.

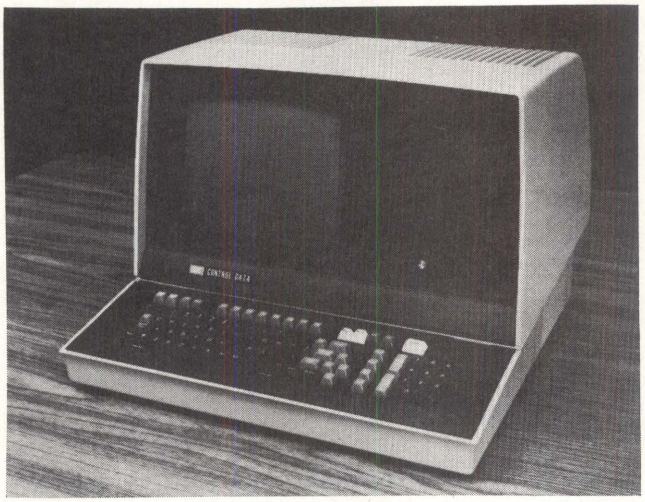
For additional information circle 199 on inquiry card.

PRODUCTS

Keyboard-Display Unit Provides Full Data Editing Capabilities

A microprocessor-controlled terminal for minicomputer systems or information terminal subsystems in which distributive processing and low cost are major concerns, the model 92456 offers local or remote data entry or editing capabilities to match its information handling environment. When used as a data entry and display element of a terminal subsystem connected to a remote computer, the unit provides full data editing capabilities at the terminal site—with resultant lower communication time charges and lower required computer resources. Cabled directly to a local minicomputer, the display receives edit commands from the host system after transmitting all keyboard operations to the computer. Up to 24, 80-char lines of data are displayed. Data are transmitted asynchronously in half- or full-duplex modes, char by char or block at a time, at speeds up to 9600 baud. 96 ASCII characters and 32 control symbols are formed in a 7 x 9 dot matrix. The detachable N-key rollover keyboard has 71 keys in the basic configuration with 13 more available in a numeric pad and 12 additional with the edit option. **Control Data Corp,** Box O, Minneapolis, MN 55440.

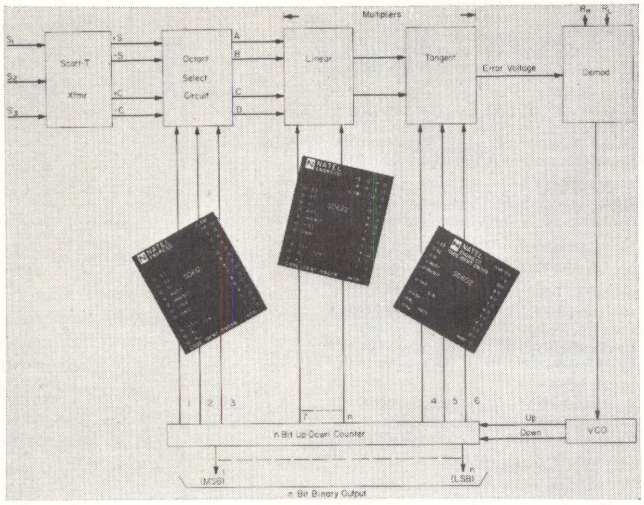
Circle 200 on Inquiry Card



Single Module Synchro-Digital Converters Have Built-In Transformer Isolation

Space, power, weight, and cost are all conserved through development of transformer isolated synchro-digital converters packaged in single, standard sized modules. Models 602, 612, and 622—with resolutions of 12, 14, and 16 bits, respectively—accept either 3-wire synchro plus reference or resolver plus reference input signals and are insensitive to voltage and frequency line variations of up to 15%. When tracking a rapidly changing angular motion, the converters have no lag and zero velocity errors up to 10,800 deg/s for the 602, 3600 for the 612, and 1000 for the 622. Accuracies are 8, 4, and 1.8 arc-min, respectively, all +0.9 LSB. The 602 measures 2.6 x 2.6 x 0.82" (6.6 x 6.6 x 2.08 cm) and works off a single 5-V supply; the 612 and 622 are 2.6 x 3.1 x 0.82" (6.6 x 7.9 x 2.08 cm) and require an additional 15-V source. (No −15-V supplies are required.) Both 0 to 70 and −55 to 105°C versions as well as high reliability devices using MIL-STD-883 components are available. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

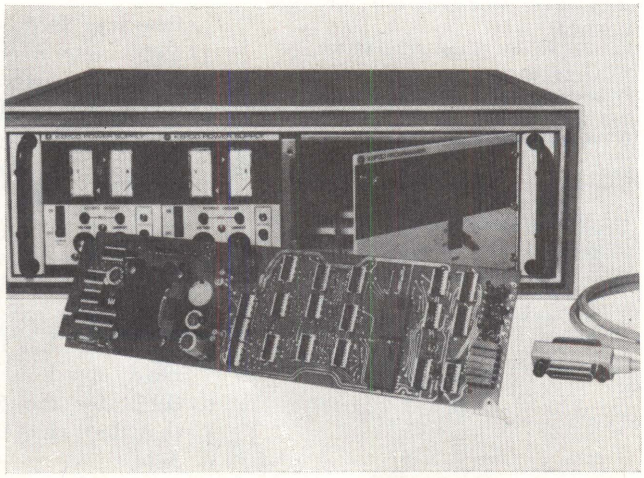
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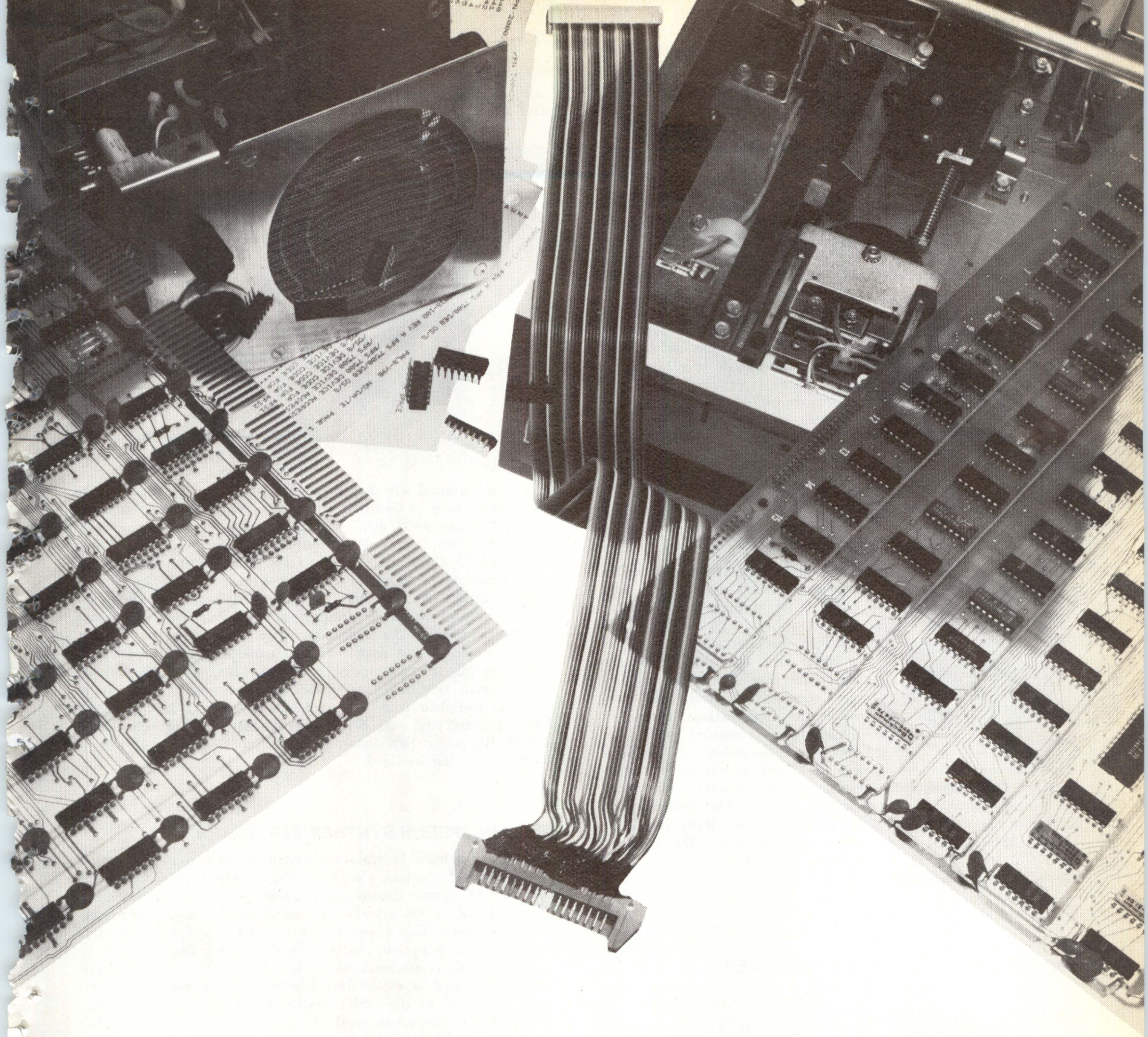


Programming System Addresses Power Supplies Through Interface Bus

System SN-488 enables any of hundreds of operationally programmable power supplies to be addressed via a general-purpose interface bus and ordered to provide programmed levels of voltage and current output. Up to eight different, isolated power supplies can be addressed through a single bus connector. Hardware consists of a card cage containing an interface card which implements the 3-wire handshake and control protocols required by the general-purpose bus. This card also performs an ASCII (8-line) to hexadecimal conversion using a ROM. Hexadecimal byte-serial output of the card is fed to an internal bus which distributes it to program cards that are in turn coupled to the internal bus through 1000-V optical isolators. Each card contains address decoding logic, storage registers, and two DACs which output low impedance analog signals. The internal bus may also be programmed by an optional hex keyboard. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.

Circle 202 on Inquiry Card



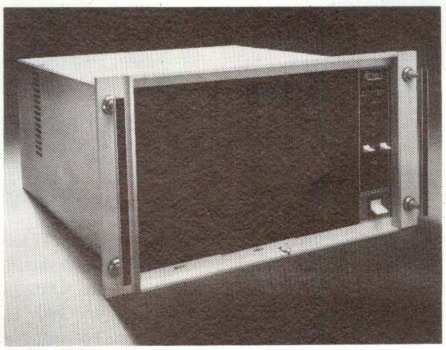


DON'T GO TO PIECES. GO TO REMEX.

A cost/effective OEM flexible disk system can't be pieced together — hardware from one source, firmware from another, software from a third. Getting optimum performance at a low unit price requires design control to eliminate redundancy and volume production to reduce cost.

That's why Remex offers the RFS7500 Flexible Disk System — a complete system designed and built by Remex — including one to four Remex drives, a microprocessor based controller/formatter, software and interfaces for most major minicomputers plus power supply, cable and rack mountable chassis. The RFS7500:

☐ expands data capacity through implementation of IBM3740 format or a user selectable 1, 2, 4, 8, 16, 26 or 32 sector format. ☐ saves computer time by data block transfer of from one to 65K 2-byte words on a single command from the host. ☐ reduces core memory requirements due to automatic track and sector search and auto-initializing without software. ☐ simplifies operation and system integration by 8-command structure. ☐ saves space by housing interface card in the system chassis in some configurations. ☐ speeds access through 6 ms track to track speed plus unit select.



Ex-Cell-O Corporation

REMEX DIVISION

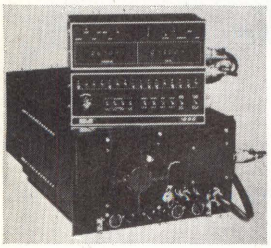
The Remex RFS7500 is a better system at lower cost than the OEM can build himself or buy from a minicomputer manufacturer or second level supplier. Don't go to pieces, go to Remex, 1733 E. Alton St., P.O. Box C19533, Irvine, CA 92713 (714) 557-6860.

CIRCLE 69 ON INQUIRY CARD

LOW LEVEL DIGITIZERS

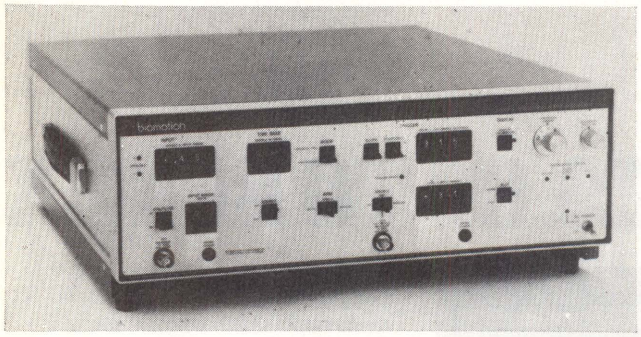
Model 100R1, one of a series of modules designed to fit directly onto the bus of the DEC LSI-11 microcomputer and PDP-11/03 minicomputer, contains a multireed, very low thermal emf, "flying capacitor" low level multiplexer that can process eight or 16 differential low level analog inputs at the rate of 200 samples/s. A software programmable range 12-bit ADC module is included. Autozeroing and six gain settings are provided in the programmable amplifier, allowing input sensitivities from 10 to 500 mV full scale. A cold junction compensation circuit that can be software programmed on a channel to channel basis to allow direct operation with all standard thermocouples is optionally available. Each unit can operate under program control or program interrupt. A 16-bit status and control register sets operating conditions. **Adac Corp,** 15 Cummings Park, Woburn, MA 01801.
Circle 203 on Inquiry Card

SEVERE-ENVIRONMENT COMPUTER SYSTEM



A model 1666 computer, which features a resource management unit (RMU) for memory mapping and protection, and an RMX/RDOS real-time disc operating system are included in a computer system designed for severe environment military command, control, and communications applications. Three processors in the computer provide for overlapped operations on separate data, executive/user operating modes, and an extensive instruction set. One processor is a g-p device that is microprogrammed for use of custom microcode, the second is a 64-bit floating point unit, and the third is for direct memory access. With the RMU, up to 1M words of memory can be addressed. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 204 on Inquiry Card

SINGLE-EVENT WAVEFORM RECORDER



Developed for scientific, engineering, and military applications, model 6500 resolves input signal levels to 1 part in 64 (6-bit resolution) and stores signal samples at sample rates from dc to 500 MHz. Samples are digitized by an input ADC and stored in a 1k-word, solid-state digital memory. Input amplifier bandwidth is dc to 100 MHz and input-voltage ranges are ±250 mV to ±5 V. Sampling rates from 2 ns to 1 s/sample (500 MHz to 1 Hz) can be selected from an internal time base, or an external time base can be input at any rate from dc to 500 MHz to synchronize the linear or sampling to other equipment in a system or to provide any desired record rates. **Biomation,** 10411 Bubb Rd, Cupertino, CA 95014.
Circle 205 on Inquiry Card

TERMINAL KIT FOR 8-BIT COMPUTERS

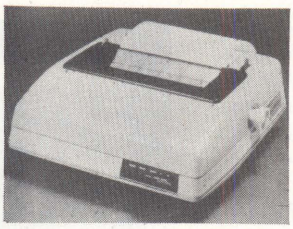


CT-64, a terminal kit that is usable with any 8-bit computer, provides 16 lines of 64 or 32 characters, complete cursor control, a full 128-char ASCII display with switchable upper or upper/lower case char, and two 1k memory pages. An optional fully assembled 9" (22.9-cm), 12-MHz CT-VM monitor with matching cover completes a full CRT terminal. The terminal offers scrolling or page mode operation, 32-control-character decoding, selectable control character printing, and char or word highlighting (with reversed background). It also provides full cursor control, home-up and erase, erase to end-of-line or end-of-frame, cursor on/off, screen reversal, scroll or page, solid or blinking cursor, page selection, and end-of-page warning beeper. It is supplied complete with keyboard, power supply, 110- to 1200-baud interface, and case. **Southwest Technical Products Corp,** 219 W Rhapsody, San Antonio, TX 78216.
Circle 206 on Inquiry Card

PLUG-IN SPEECH SYNTHESIZER BOARD

Sounds are defined in real time under software control with the model CT-1 synthesizer. Parameters which represent the phonetic structure of human speech are transmitted to the synthesizer at a rate of 500 to 900 bytes/s, depending on the data compression techniques used. This allows production of intelligible and natural sounding speech output. Speaker characteristics and language or dialect variations are retained in the output. The synthesizer can also be operated in a low data rate mode using phoneme definitions contained in the CSR1 synthesis-by-rule software package. The software driver can easily be modified to keep the naturalness and intelligibility of the speech output up to date. **Computalker Consultants,** PO Box 1951, Santa Monica, CA 90406.
Circle 207 on Inquiry Card

BELT-IMPACT LINE PRINTER



Price competition with dot-matrix and other serial printers is attained in the desktop model 10 by use of a belt-impact print mechanism that enables 150-line/min printout with a full 64-ASCII char set in 80-col format. Both friction and pin feed versions are available. Print rate with a 96- or 128-char set is 84 to 110 lines/min. Interface is 8-bit parallel TTL level, Centronics-compatible. An RS-232-C serial interface is optionally available. Data input rate is 75k char/s max. Voltage requirements are 100/115 or 220/240 Vac ±10% 50/60 Hz, single phase; power consumption is 150 W max. **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505.
Circle 208 on Inquiry Card

Now there's an alternative to the high cost of mainframe disc storage. DIVA's Computroller V.

If you've decided to buy your minicomputer system from DEC, DG or Interdata, you already know the facts about their disc storage systems. They're well designed. They're also expensive.

Now, you can get the same high performance, reliability and software transparency of the mainframe product at a price that makes sense. With Diva's Computroller V line of disc systems.

The Computroller V matches the mainframer's system feature-for-feature, but costs up to 50 per cent less to purchase, install and maintain. With no shortcuts in design or service support.

The reason? Unlike the mainframer, we specialize in the development of disc storage systems to help you cope with the continuous expansion in information processing. The Computroller V has an amazing capacity range of 25-300 megabytes per spindle. Plus compatibility with the mainframe system and total software transparency.

No other disc storage system can interface, adapt and self-test like the Computroller V. Make your own comparison and see how the Computroller stacks up against other mainframe products.

	DIVA Computroller V	Mainframer
Complete Software Transparency	YES	YES
ECC Error Correction	YES	YES
Complete Customer Services	YES	YES
Resident Self-Checking Diagnostics	YES	YES
Microprocessor Technology	YES	YES
Dual Processor Support	YES	YES
Interface to Most 3330 Technology Drives	YES	NO

From now on, this may be the only system your company will need for mass storage. For more information, fill in the coupon or call Toll-Free at 800-631-2141.

DIVA, Inc./ Dept. **A2/607** Industrial Way West/ Eatontown, New Jersey 07724

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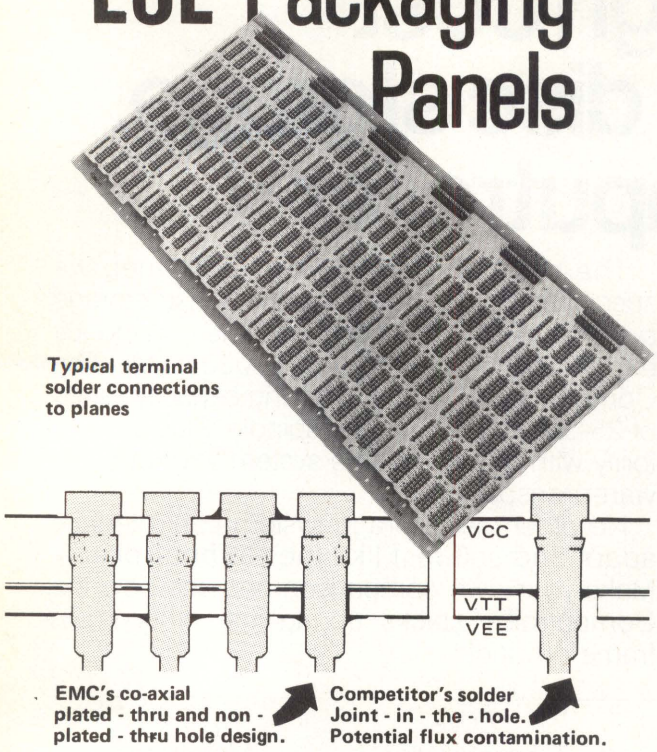
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CIRCLE 70 ON INQUIRY CARD

ECL* Packaging Panels



*Eliminate Contaminated Layers

Packaging panels for ECL do work!

Typical of EMC . . . a clever, unique solution to an annoying problem. Soldering terminals to the top (VCC) and bottom (VEE) voltage planes is easy, but reaching the middle (VTT plane) requires an enlarged hole through the bottom plane. Result? The inconvenience of working in a confined recessed hole, contamination caused by flux entrapment, and the difficulty of inspection.

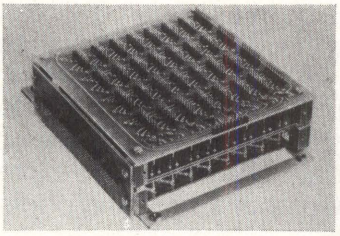
EMC solves the problem by selective plating thru of the holes needed to reach the middle plane, so that the soldering job is on the surface . . . simple, clean, easy to check. And it's ideal for installing decoupling capacitors, too. EMC's design also provides maximum metal plane coverage, and of course, uses the patented Nurl-loc terminal. Interested? Contact Electronic Molding Corp., 96 Mill Street, Woonsocket, R. I. 02895. (401) 769-3800.

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PRODUCTS

COMMUNICATION MASS SWITCHES

Designed for varied applications, mass switches based upon the company's Mini Memory matrix provide high speed switching coupled with the reliability of glass-sealed dry reed contacts. They are available in two compact sizes: an 8-relay package is 5 x 5 x 2" (12.7 x 12.7 x 5 cm) and will switch up to 32 signal input lines to any one of eight groups of 32 signal lines; a 4-relay, 2.5 x 6 x 2" (6.35 x 15.24 x 5 cm) unit will switch up to 32 signal input lines to any one of four groups of 32 signal output lines. Contact ratings are: power, 5 VA max switched; voltage, 250 Vac max switched; current, 0.5 A max switched and 1 A max carry only; resistance, 100 mΩ max independent inputs and outputs, 200 mΩ max bused inputs or outputs. Set and reset pulse durations are 0.5 ms min with 1.0 ms recommended. **C. P. Clare & Co,** 3101 W Pratt Ave, Chicago, IL 60645.
Circle 209 on Inquiry Card

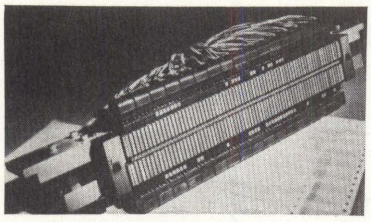


LOW COST LABORATORY COMPUTER SYSTEM

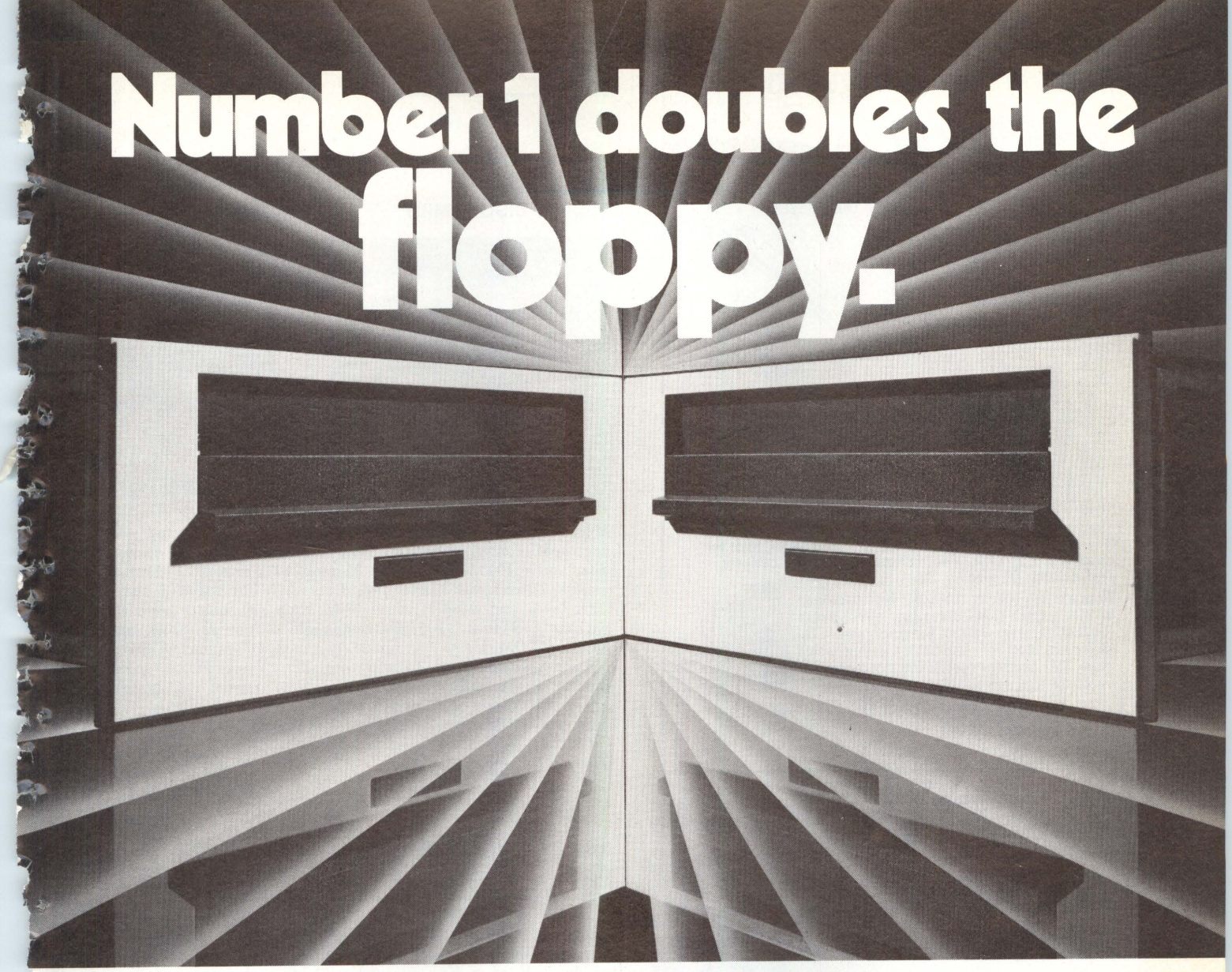
Up to 15 industry std lab devices can be supported on the DECLAB-11/03 IB, which incorporates a PDP-11/03 microcomputer and an instrument bus based on IEEE Standard 488-1975. The system employs FORTRAN IV programming language and the RT-11 operating system. A scientific subroutine package is supplied for analyses of data from instrumentation, through user-developed software handlers. Two versions of the system are available: one uses an LA36 teleprinter as a system terminal, the other employs a VT55 video graphics terminal. Both have floppy-disc storage and can be used either in standalone mode or as part of a computer hierarchy. Optional interfaces for the system include A-D and D-A converters, parallel digital input and output interfaces, and a programmable real-time clock. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 210 on Inquiry Card

PRINT HAMMER MODULES

Proprietary Mark IV print hammers, used in the company's line printers, are being made available to manufacturers of many other types of printers. Demonstrated MTBF of the hammers is 4 x 10^9 impacts. Hammers will be supplied either individually or in std or custom banks. Engineering assistance will be provided for putting together custom hammer-banks. Hammer impact is actuated by a current that flows through a flat voice-coil mechanism. The hammer tip is mounted on top of the coil, and this assembly is suspended by two flex-pivot springs which also serve as the current path to the coil. A current in the coil, which is placed between permanent magnets, produces a force that causes the hammer to impact the paper, ribbon, and character. **Data-products Corp,** 6219 De Soto Ave, Woodland Hills, CA 91364.
Circle 211 on Inquiry Card



Number 1 doubles the floppy.



Doubled data storage capacity. Doubled access speed. Doubled floppy media selection. Get it all with the new Shugart double-sided single/double density floppy disk drive. All this for only 25% more than a single-sided floppy.

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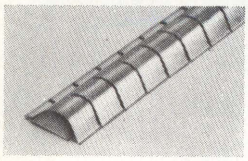
Number 1 in low cost disk storage.

Shugart Associates®

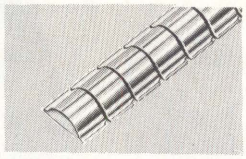
CIRCLE 72 ON INQUIRY CARD

When RFI problems get sticky, try Sticky Fingers®

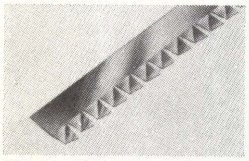
Attaches faster, shields better than anything else!



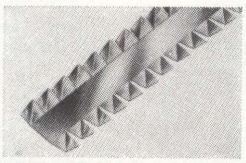
SERIES 97-500 The original Sticky Fingers with superior shielding effectiveness.



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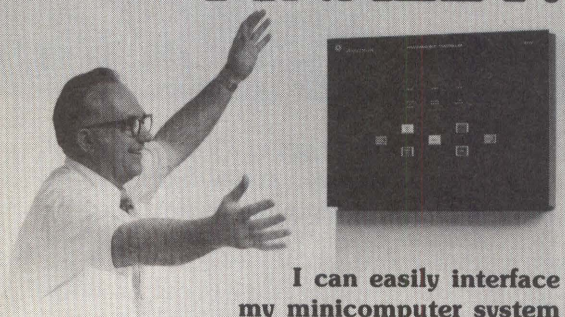
Now you can specify the exact type beryllium copper gasket that solves just about every RFI/EMI problem. Perfect for quick, simple installation; ideal for retro-fitting. Self-adhesive eliminates need for special tools or fasteners. Write for free samples and catalog.



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With the 8500, your minicomputer system can interface directly to the Byte Mux, Block Mux, or selector channel.

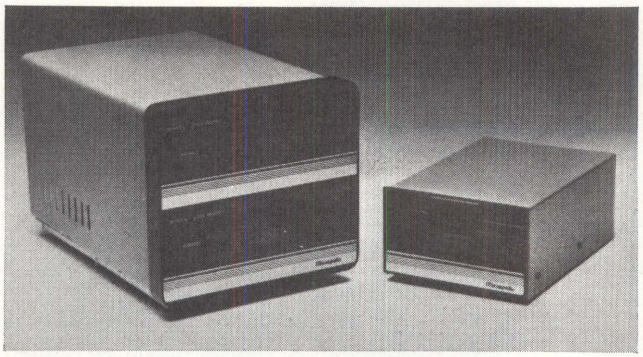
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CIRCLE 74 ON INQUIRY CARD

PRODUCTS

FLOPPY DISC FAMILY



MetaFloppy units are designed to provide performance and storage capacity of 8" (20.32-cm) discs in a 5.25" (13.34-cm) format. Single-drive 1043-Mod I uses a 35-track, 143k-byte disc; -Mod II uses a 77-track, 315k-byte disc. Dual drive 1053-Mod I stores 286k bytes, and -Mod II stores 630k. Each system is a complete package including S-100/8080-compatible controller, cables, and autoload ROM. Up to four single, two dual, or any mix of drives can be accommodated by the controller. Track-to-track access time is 30 ns; settling time is 10 ns; data transfer rate is 250k bits/s. Error rate is 1 in 10^9 bits. Disc operating life is $>10^6$ passes/track. **Micropolis Corp,** 9017 Reseda Blvd, Northridge, CA 91324.
Circle 212 on Inquiry Card

0.6-IN³ SOLID-STATE RELAY

Despite its 0.475" (1.2-cm) height, which allows mounting on racked PCBs, Micro Cube has a switching capability of 2.5 A at 25°C, is optically isolated, can withstand 400-V transient pulses, and has a 3000-V/μs dV/dT rating. It is optically isolated and includes a zero voltage turn-on circuit which operates within 7 V of a Vac alternation. Additional features include 1500-Vac dielectric strength and the ability to withstand 100 A of surge current for one cycle. The unit requires no additional heat sinking at its catalog ratings. Its input circuit operates on 3 to 15 Vdc and is compatible with logic circuitry. A 14- to 30-Vdc control voltage range is available as an option. Termination is on 100-mil centers. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.
Circle 213 on Inquiry Card

PROGRAMMABLE TERMINAL SYSTEMS

Elite 4000A, a flexible, modular computing system with an 8-bit word length, features block-oriented display organization for fast insertion, deletion, or rearrangement of text; interrupt driven vectored I/O; direct memory access capability; 8-level video (reverse, half-intensity, blink); stored memory tag bits; expandable display memory (to 32k); expandable I/O; expandable character set; and switch-selectable soft/hard keyboard. Use of a microprocessor in the design provides flexibility in display formatting, text editing, and data collection and processing.



Datamedia Corp, 7300 N Crescent Blvd, Pennsauken, NJ 08110.
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ok wire wrapping center ok

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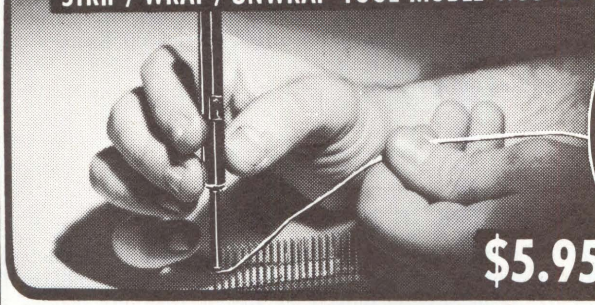
1

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STRIP / WRAP / UNWRAP TOOL MODEL WSU-30



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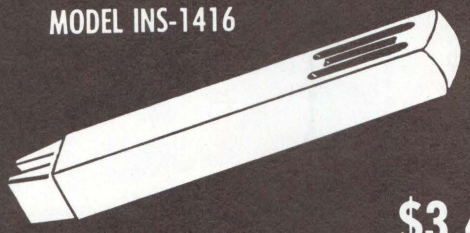
WIRE DISPENSER MODEL
WD-30-B



THE DISPENSER WHICH CUTS AND STRIPS THE WIRE

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DIP IC INSERTION TOOL WITH PIN STRAIGHTENER
MODEL INS-1416



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5

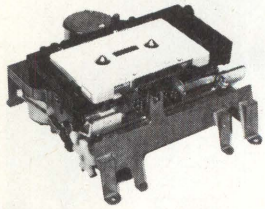
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* MINIMUM ORDER $25.00, SHIPPING CHARGE $1.00, N.Y. CITY AND STATE RESIDENTS ADD TAX

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CIRCLE 76 ON INQUIRY CARD

IEEE MEMBERS

You have a stake in your profession. IEEE's Board of Directors has nominated a person who is president of a large corporation ($10⁸ sales, 3100 employees) and who has not been involved in professional activities. By contrast, Irwin Feerst is a working engineer who has brought to IEEE's attention

the practice of mandated, built-in, unpaid overtime;

the counter-productive recruiting efforts by the academics;

the false manpower projection figures which always predict a shortage of engineers.

VOTE FOR

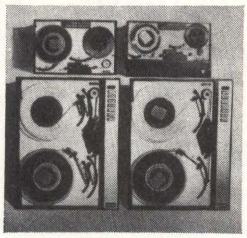
IRWIN FEERST

for IEEE President

(For sample copy of newsletter devoted to the interests of the working EE, circle number 77)

PRODUCTS

7 AND 8½" MAGNETIC TAPE DRIVES

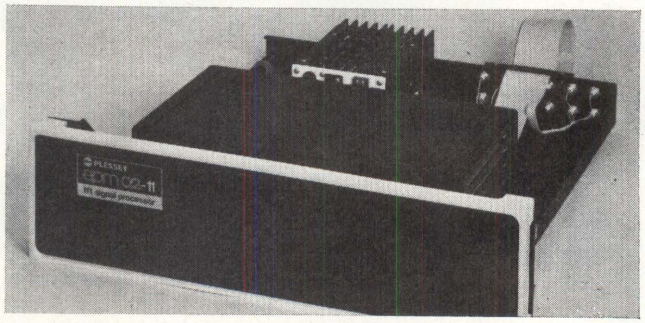


Model 70X and 80X, for 7 and 8½" reels, respectively, feature spares commonality of the head, tape guiding hardware, EOT/BOT, file protect, control switches, and electronics, and a common universal dual density read/write board which enables NRZI, PE, or both and is pluggable for any speed from 12.5 to 75 in/s (31.75 to 190.5 cm/s). These and all other members of the series X magnetic tape drive family feature direct drive motors and dual formatting. In addition, the 70X features speeds from 12.5 to 37.5 in/s (31.75 to 95.25 cm/s). **Cipher Data Products, Inc,** 5630 Kearney Mesa Rd, San Diego, CA 92111.
Circle 215 on Inquiry Card

PYROELECTRIC IR DETECTOR

Model 406 consists of a sensing element and a complete impedance converting source follower/voltage mode amplifier. The converter changes high impedance signals from the sensing element into low impedance voltage signals. Sensing element and the integrated electronics are electrically floating within the detector housing. The housing is connected to a separate pin. A Germanium window, which can be supplied at no extra cost, is required to hermetically seal the sensing element and electronics against contamination, physical damage, visible light, and electrical noise. This window provides max transmittance for 3- and 10.6-μm wavelengths. Detector dia is 2 mm, voltage responsivity (at 10 Hz) is 275 V/W, and optical bandwidth is 2 to 15 μm. **Eltec Instruments, Inc,** PO Box 9610, Daytona Beach, FL 32020.
Circle 216 on Inquiry Card

FFT ADD-ON PROCESSOR



A peripheral for use with DEC PDP-11 minicomputers and the LSI-11 microcomputer, the SPM 02-11 fast Fourier transform module provides a high speed processing capability as a low cost function. It is capable of transforming 1024 complex points in 237 ms and can operate on transform sizes varying from eight to 1024 complex points. The unit operates with its own memory and processes data independently of the host minicomputer, with all data transfers taking place under DMA, so that it does not impede operation of the host minicomputer. Data to be processed may either be supplied in digital format from the host machine or be directly sampled via an integral 12-bit ADC. A 12-bit DAC is included to transform data for viewing on an oscilloscope. **Plessey Microsystems,** Water Lane, Towcester, Northamptonshire NN12 7JN, England.
Circle 217 on Inquiry Card

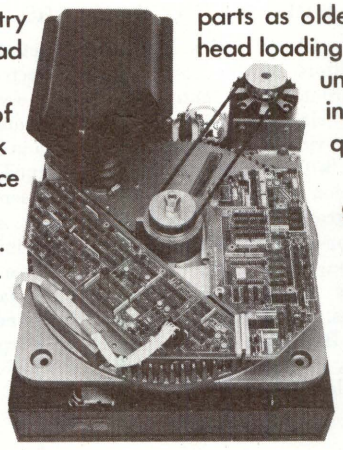
Another first for ISS

THE INDUSTRY'S MOST ADVANCED FIXED HEAD DRIVE

Announcing another in a long line of industry firsts for ISS—the ISS 550—the first fixed head disk drive to employ Winchester technology.

ISS is not only an innovator, but also one of the world's foremost manufacturers of OEM disk products, with all that means in the way of service back-up, spares, and technical assistance.

But at ISS, being first alone is not enough. The new ISS 550 has truly outstanding performance. Field upgradable capacity from 12.8 to 51.2 megabits. Average access time of 8.3 milliseconds. Sector formatting to meet individual requirements. And advanced technology that results in extremely low error rates.



Data transfer rate is 12MHz, and if that's too fast, you can slow it down with our data rate buffering feature.

But even high performance isn't everything. The new 550 is exceptionally reliable. It has only 25% as many parts as older technology fixed head drives. There's no head loading mechanism. DC power supply is built in. The unit is self clocked. And the design incorporates interchangeable modular subassemblies for quick and easy maintenance.

All this performance and all this reliability go into a compact package that occupies just 14.5 inches of rack space.

But when all is said and done, the most significant statement we can make about the 550 is this: the price-performance ratio is twice as good as that of fixed head drives using older technology.

Get full details on this ISS first. ISS is an operating unit of Sperry Univac bringing technological leadership for the generations ahead. Write or call OEM Marketing, ISS, 10435 N. Tantau Avenue, Cupertino, California 95014, Telephone (408) 257-6220.

ISS 550. Twice the peformance.

SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORPORATION

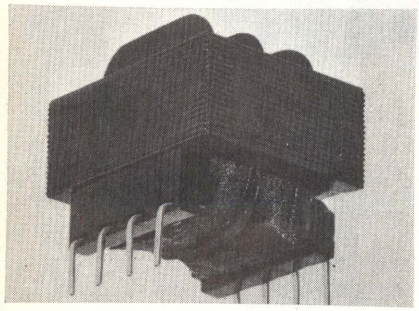
CIRCLE 78 ON INQUIRY CARD

PRODUCTS

INSTRUMENT STEPPING MOTOR

Available with gear head or direct drive, model AB is of permanent magnet construction with standard rotor speeds of 6, 10, 12, 20, 30, 60, 120, and 600 r/min (direct drive). Torque examples are 88 oz-in at 10 r/min, 29 oz-in at 30 r/min. Gear-train rating is 150 oz-in (1.05 N•m) at 1 r/min. Hardened steel, broached gears, and heat-treated steel pinions assure troublefree gear-train operation. The motor is electrically reversible, simply by changing one connection. All motors are supplied with capacitors. **Hurst Mfg Corp,** Princeton, IN 47670.
Circle 218 on Inquiry Card

PCB TRANSFORMERS



Split/Tran[R] miniature PC board transformers use a split bobbin winding concept to provide high isolation (2500 V rms HIPOT std) and low capacitive coupling, eliminate the need for electrostatic shielding, and offer significant reductions in size and weight. The line is available with single 115-V or dual 115/230-V primaries; secondaries are split to permit series or parallel connection. Std units range from 2 to 20 VA; all have PC pins ready for insertion into boards. **Signal Transformer Co, Inc,** 500 Bayview Ave, Inwood, NY 11696.
Circle 219 on Inquiry Card

MICROPROCESSOR EVALUATION BOARD

A complete evaluation board designed to test the Texas Instruments TMS-9900 chip, the package includes components, listing of the monitor, and design documentation for the appropriate microcomputer kit. Wirewraps interconnecting all components have been made on a single 9.75 x 9.25" (24.77 x 23.5 cm) board, which saves significant manhours in design, interconnection, and evaluation of the chip. The board can be easily modified to accommodate any circuit change. **Cambridge Thermionic Corp,** 445 Concord Ave, Cambridge, MA 02138.
Circle 220 on Inquiry Card

SATCOM FREQUENCY CONVERTERS

Series UC/DC family has been expanded with models UC6-D2/D2 and DC4-D2/D2, designated for PSK/QPSK data carriers such as Intelsat SCPC, SPADE, high speed digital facsimile, and other 6/4-GHz domestic and international satellite data transmission applications from 48k to 10M bits/s. Optimized for high frequency stability and spectral purity, the units assure low bit error rates in data communications service, and feature 4-channel switchability, crystal-controlled, with an external synthesizer input for interim frequency assignments. **LNR Communications, Inc,** 180 Marcus Blvd, Hauppauge, NY 11787.
Circle 221 on Inquiry Card

16-CHANNEL DATA ACQUISITION SYSTEM

ZMP 1000, a self-contained data acquisition system offering 12-bit resolution, is capable of multiplexing 16 channels of real-time physical data from sensors and converting them to digital information. Monotonicity is guaranteed over the full 0 to 70°C op temp range. A-D conversion time is 12 μs max, adjustable to throughput rates up to 50,000 channels/s. Sixteen single-ended, 16 pseudo-differential, or eight true differential inputs are provided. Differential linearity is $<\pm 1$ LSB with no missing codes. **Zeltex, Inc,** 940 Detroit Ave, Concord, CA 94518.
Circle 222 on Inquiry Card

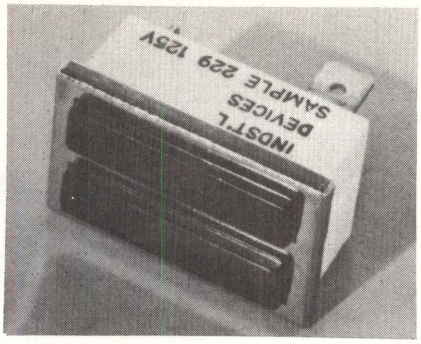
7 X 9 DOT MATRIX MONITORS

TTL-120/150 series TTL-level direct drive monitors provide capability for electronic horizontal video centering within the raster, and electronic vertical linearity control. Fine video adjustments can be made rapidly without disturbing factory-aligned deflection components. Simple subassembly interconnection allows a modular sync stripper board for EIA composite inputs to be added as required. Performance options include high line rates, dynamic focus, and skip-scan features. **Ball Brothers Research Corp, Electronic Display Div,** PO Box 3376, St Paul, MN 55165.
Circle 223 on Inquiry Card

20-CONTACT SOCKET STRIPS

Available in 20-contact lengths with choice of wirewrap, solder-pin, or solder-shell termination styles, all strips feature "easy-instant-breakaway" for snapping strips into shorter length with no tools or cutting. Mating male-pin terminal strips feature solder-pin, solder-pot, or solder-head connections. All sockets/terminals are on 0.100" (0.254-cm) space in-line; strips mount 0.100" (0.254-cm) spacing side-by-side to form 0.100" (0.254-cm) grid patterns. Strip is glass-filled polyester. **Samtec, Inc,** 810 Progress Blvd, New Albany, IN 47150.
Circle 224 on Inquiry Card

DUAL-LAMP INDICATOR LIGHTS



Providing two rectangular bars of light, with imprinted legends when desired, in a variety of lens color combinations, series 2350 features two full-width 1.156 x 0.25" (2.94 x 0.64 cm) over-and-under lenses; series 2320 has two 0.56 x 0.25" (1.42 x 0.64 cm) side-by-side lenses. Indicators snap-fit into rectangular openings in panels up to 0.156" (3.96 mm) thick. Units are available with three leads or three terminals (one common) or four leads for two separate circuits. Lamps can be lighted individually or simultaneously. **Industrial Devices, Inc,** 7 Hudson Ave, Edgewater, NJ 07020.
Circle 225 on Inquiry Card

MICROCOMPUTER POWER SUPPLIES

Series 1000 microhybrid power supplies designed to interface with microprocessor-based systems is comprised of three models that use single, dual, and triple outputs in combinations to power analog I/O boards, microcomputers, and microhybrid systems. Operating features include dual-tracking output voltages, output current limiting, and 0.5% output voltage adjustments by means of externally accessible trimmer potentiometers. 5-V outputs have built-in overvoltage protection as std. Units operate from 115 V, 50-400 Hz with no derating. **SGR Corp,** Neponset Valley Industrial Pk, PO Box 391, Canton, MA 02021.
Circle 226 on Inquiry Card

DISPLAY OSCILLOSCOPE

Model 4061 magnetically-deflected oscilloscope utilizes a 9" (22.8-cm) diag CRT. Its open frame aluminum chassis measures 7 x 10 x 9" D (17.8 x 25.4 x 22.9 cm) and holds a PC board with control circuitry and plug-in connections for direct interface with the user's equipment. Protection circuitry automatically causes the intensity to decrease to nondestructive level after a 6 (± 4) s loss of horizontal control. Scope has a 15-kHz bandwidth vertically (Y input) and 4-kHz horizontally (X input). Sensitivity is 5 V for 4.3" (10.9 cm) of vertical and 6.2" (15.7 cm) of horizontal deflection. **Telonic Altair,** 2825 Laguna Canyon Rd, Box 277, Laguna Beach, CA 92652.
Circle 227 on Inquiry Card

OEM America Meets

at the Invitational Computer Conferences



In Boston... in Houston... in Orange County, and in six other cities, OEM decision-makers meet the country's top computer and peripheral manufacturers at the Invitational Computer Conferences—the only seminar/displays designed specifically for the unique requirements of the quantity user.

In one day, at each 1977/78 ICC, guests will receive a concentrated, up-close view of the newest equipment and technology shaping our industry. Some of the companies which participated in the 1976/77 Series were:

Amcomp, Ball Computer, Braemar Computer, Calcomp, Centronics, Cipher Data, Computer Automation, Computer Operations, Control Data, DEC, DIVA, Data 100, Data Systems Design, Dataflux, Dataram, Diablo Systems, Digi Data, EECO, Florida Data, General Automation, General Instruments, Hazeltine, Hewlett Packard, Honeywell, Houston Instrument, ISS/Sperry Univac, Interdata, Kennedy, Lear Siegler, MDB Systems, Microdata, Mohawk Data Sciences, Monolithic Systems, Omron, PerSci, Pertec, Pioneer Magnetics, Plessey Microsystems, Printronix, Remex, Shugart Associates, Tally, Tandberg Data, Tektronix, Threshold Technology, Tri-Data, Varian Graphics, Wangco, Xylogics.

The Schedule for the 1977/78 Series is:

September 7, 1977 Newton, Mass.
October 4, 1977 Minneapolis, Minn.
October 27, 1977 Palo Alto, CA.
November 17, 1977 Houston, Texas
January 19, 1978 Orange County, CA.
February 2, 1978 Ft. Lauderdale, Fla.
March 2, 1978 St. Louis, Mo.
April 4, 1978 Hasbrouck Heights, N.J.
April 6, 1978 Valley Forge, PA.

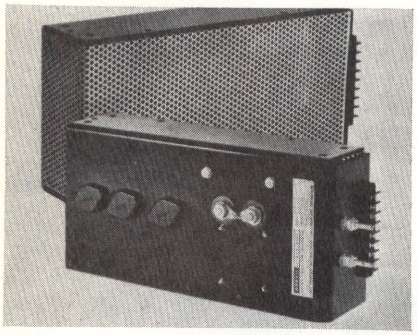
Invitational Computer Conferences

Invitations are available from participating companies or the ICC sponsor. For further information contact: B.J. Johnson & Associates, 2503 Eastbluff Drive, #203, Newport Beach, Calif. 92660 (714) 644-6037.

CIRCLE 79 ON INQUIRY CARD

PRODUCTS

SWITCHING REGULATED POWER MODULES



Each unit of the DA100 series is operable from user selectable inputs of 115 Vac ±10% 1ϕ or 3ϕ Wye, or 230 Vac ±10% 1ϕ or 3ϕ Delta. Three units are available with outputs of 5, ±12, and 15 Vdc with total power of 100 W. Full power at ambient temp of 55°C with 50% derating at 71°C is also available. Line and load regulation is <0.5% and pk-pk ripple is <100 mV. Overvoltage and short-circuit protection, overtemp shut-down, and remote error sensing are std. **Abbott Transistor Laboratories, Inc,** 5200 W Jefferson Blvd, Los Angeles, CA 90016.
Circle 228 on Inquiry Card

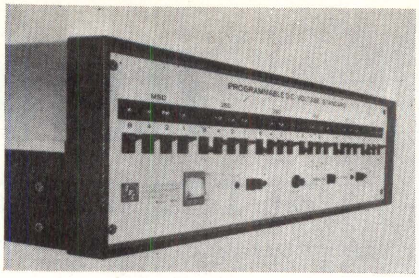
DISC DRIVE CLOCKWRITER

A clock and sector track writer designed to write the fixed head timing track on the 3350 Winchester-type disc memories is one model of the PM 2390 series. Unit features a super-smoothing technique which allows the writing of a closed clock track at rates up to 24M bytes/s, having undetectable closure error with negligible jitter or phase shift. The instrument can write custom sector and address patterns, and open clocks with a gap length up to 100 ms. It measures frequencies to 25 MHz, and amplitude and/or frequency modulation. **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.
Circle 229 on Inquiry Card

0.3" HIGH LED DISPLAYS

HERCULES LEDs are available in models 1737 through 1739. The 1737 is common anode with right- and left-hand decimal; 1738 is common cathode with right-hand decimal; and 1739 is common anode with ±1 overflow indicator. All have red character appearance and uniform segments with high contrast and wide viewing angle. Displays feature std 0.3" (7.6-mm) DIP LED configuration to PC board or std socket mountings. They are categorized for luminous intensity and are IC compatible. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.
Circle 230 on Inquiry Card

DIGITALLY PROGRAMMABLE STANDARD

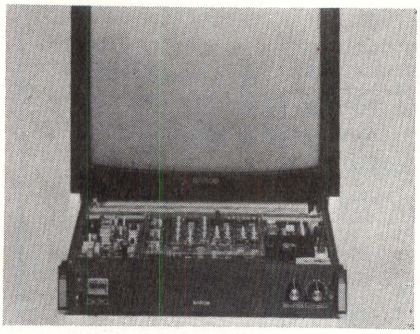


Designed for high speed and flexibility, the 501 system is suited for automated production line testing and QC, testing for response time, linearity, accuracy, threshold levels, and, for amplifiers, gain characteristics. Features include 50-μs switching and settling time; BCD programming 8421 or ASCII; binary; TTL compatibility; and high accuracy NBS traceability. With options, unit becomes a total system with 1-μV to 200-Vdc output, resolution of 0.1 μV (1 ppm), and speeds of 50 to 500 μs. **Electronic Development Corp,** 11 Hamlin St, Boston, MA 02127.
Circle 231 on Inquiry Card

15-DEG ANGLE STEPPER MOTORS

Series 10,000 variable reluctance motors provide a 15-deg step angle. In a 2.000" (5.08-cm) dia housing, the units have 3- or 4-phase windings and can be supplied with a variety of lead screw shafts. Devices are rated at 24 steps/rev with ±3% step accuracy. Holding torque is 35 oz-in (0.245 N•m) 3-phase, 40 oz-in (0.28 N•m) 4-phase; running torque is 14 oz-in (0.10 N•m); and rotor inertia is 10 gm•cm^2. **Transicoil, Inc, Commercial Products Div,** Worcester, PA 19490.
Circle 232 on Inquiry Card

COLOR CRT DATA DISPLAY

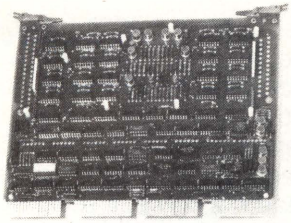


Operating at 875 lines/50 Hz, instead of the normal 625 lines/50 Hz, display takes full advantage of high resolution CRT in both the horizontal and vertical sense. CDCT/HIREM/875 data display has screen sizes of 14" (35 cm) or 20" (51 cm). High precision convergence circuitry enables information capacity of 4k char for 14" unit and 6k char for 20" version. **Barco Electronic,** Noordlaan 5, B-8750, Kuurne, Belgium.
Circle 233 on Inquiry Card

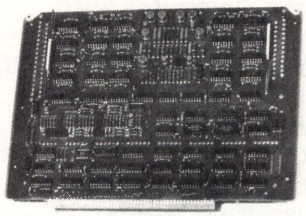
MICROPROCESSOR CORE MEMORIES

FOR THE LSI-11, 8080, 6800, IMP-16P

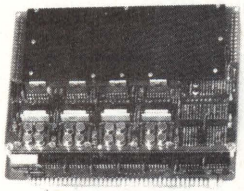
- NON-VOLATILE.
- PIN-TO-PIN COMPATIBILITY.
- POWER MONITORING FOR DATA PROTECTION.



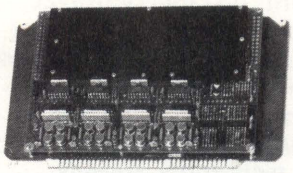
MM-16P 8K x 16



MM-1103 8K x 16



MM-6800 8K x 8



MM-8080 8K x 8

MM-1103 —Plugs directly to DEC LSI-11 and PDP 11-03 computer.
MM-8080 —Plugs directly to Intel's MCS 8 and MCS 80 Microcomputer.
MM-8080A—Plugs directly to Intel's MDS 800 and SBC 80/10 Microcomputer.
MM-6800 —Plugs directly to Motorola's EXORciser and compatible with the Evauation Modules.
MM-16P —Plugs directly to National's IMP-16P Microcomputer.

micro memory inc

9438 Irondale Ave., Chatsworth, California
Tel: (213) 998-0070

CACHE ENHANCEMENT FOR MINICOMPUTER

A high speed bipolar memory which allows rapid access to 1000 words of the main memory of the militarized PDP-11/34M minicomputer, the enhancement is available in the full ATR version of the computer. It increases throughput up to 100%. Memory has a 250-ns cycle time, byte parity, is compatible with the floating point option, and is completely transparent to the programmer. Additional benefits are that it has registers for maintenance mode, and is contained on one plug-in double module. **Norden, div of United Technologies,** Norwalk, CT 06856.
Circle 234 on Inquiry Card

DC MOTOR SPEED CONTROL



Paratrol S, an SCR control for dc motors offers speed regulation precise enough to maintain speed within 1% of its setting. Speed is adjustable over a 60-to-1 range. Models for 0.125, 0.25, 0.33, and 0.5 hp operate from 115 V, 50 or 60 Hz; 0.75- and 1-hp units are available in a choice of 115 or 230 V; and 1.5- and 2-hp models operate on 230 V. Two versions are single-direction with magnetic start/stop and magnetic reversing units with dynamic braking. **Parametrics,** 284 Racebrook Rd, Orange, CT 06477.
Circle 235 on Inquiry Card

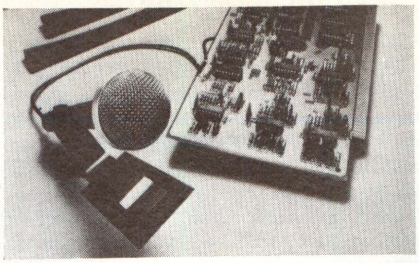
MULTIPLE-OUTPUT UPS

Expanded UPS family float charges either a 12- or 24-V backup battery and offers the choice of ±12- or ±15-Vdc output for powering analog circuits. Third output, 5 Vdc for powering logic, remains unchanged. Systems boast MTBF of >50,000 h at 25°C. Key feature is efficiency of analog and digital power sources. The units conserve battery charge by employing two forms of conversion: a high performance dc-dc converter and a high efficiency switching regulator. Voltage/current ratings for the three outputs are fixed. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.



Circle 236 on Inquiry Card

VOCAL INPUT SYSTEM



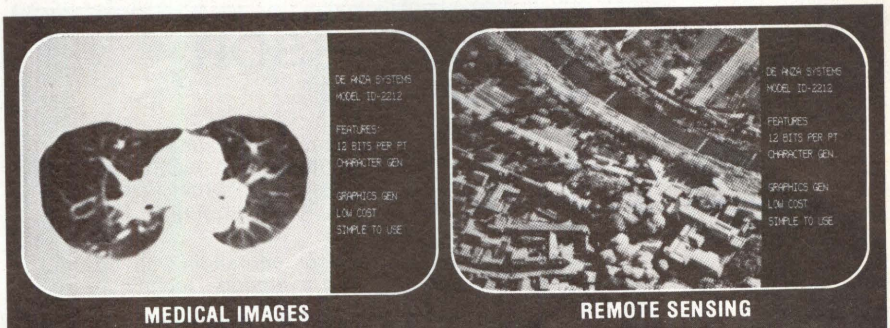
A system compatible with all S-100 bus computers to provide voice input and control is available in kit form or assembled and tested. SpeechLab™ digitizes and extracts data from a speech waveform and applies pattern matching techniques to recognize vocal input. It can be used with any computer with the aid of a separate power supply and connector. Included are a complete hard/software system, lab and hardware manuals, high fidelity microphone, and three programs on paper tape. System features 64 bytes of storage/spoken word and a vocabulary of up to 64 words in memory. **Heuristics, Inc,** 900 N San Antonio Rd, Los Altos, CA 94022.
Circle 237 on Inquiry Card

MICROPROCESSOR-COMPATIBLE DPMs

Three models of the series VII, 3½-digit panel meters are designed for system applications, offering bipolar input, rejection of common and normal mode signals, true autozero, polarity indication, selectable decimal point, 1000M Ω input impedance, and ratiometric operation. Model 70 operates from ±5-Vdc logic power input; model 75 operates from 115- or 240-Vac line power input. Both have 0.5" (1.27 cm) LEDs. Model 78 operates from 115- or 240-Vac line power input and has 0.8" (2.03-cm) LEDs. Sixty instrument configurations are possible. **Fairchild Camera and Instrument Corp, Instrumentation & Systems Group,** 1725 Technology Dr, San Jose, CA 95110.
Circle 238 on Inquiry Card

MICROPROCESSOR ALPHANUMERIC DISPLAY

DL-1416 display is fully buffered and has built-in ASCII decoder, multiplexer, memory, and LED drivers. Display creates all 64 ASCII characters 0.16" (0.406 cm) high and has high contrast and crisp appearance. It is actuated by TTL logic levels and requires only ±5-V power supply. Each 1 x 1.2" (2.54 x 3.048 cm) module displays four characters and may be butted end-to-end to create displays of any length with equal spacing between char. Any character position may be accessed independently and asynchronously. **Litronix,** 19000 Homestead Rd, Cupertino, CA 95014.
Circle 239 on Inquiry Card



MEDICAL IMAGES REMOTE SENSING

De Anza Systems New ID 2000 Series

Provides you with a low cost solution to your Image Enhancement and Processing Needs.

Take your choice... We have Systems with 256, 1024, or 4096 levels of intensity, in color or grey scale, with or without Intensity Transform Tables. Options provide interactive cursors and cursor controls, overlays and interfaces to most minis.

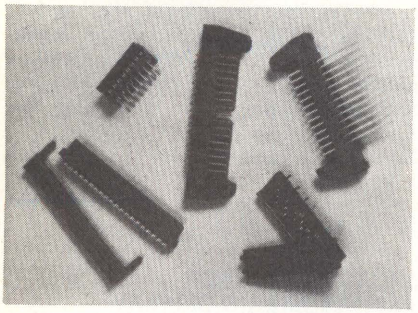
We have a lot more to say to the world of Image Processing ...and it's all worthwhile.

De Anza Systems Incorporated

3444 De La Cruz Blvd.
Santa Clara, CA 95050 (408)988-2656

PRODUCTS

10-PIN FLAT-CABLE CONNECTORS



Additions to connector line include 10-pin connectors and sockets (female sockets, PCBs, headers in both straight and right-angle versions with solder or wirewrap pins) either with or without strain relief. Connectors are also available for DIPs. Female connector caps are made from Lexan™, which permits them to be pried off and reused without danger of breaking. Connector design enables cable to be crimped onto connector prior to snapping on the cover, allowing visual inspection during the assembly process. **Alpha Wire Corp,** 711 Lidgerwood Ave, Elizabeth, NJ 07207.
Circle 240 on Inquiry Card

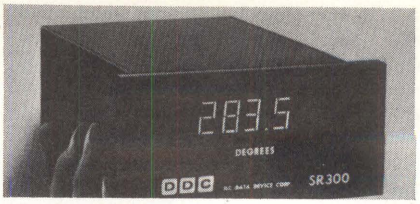
MINIATURE 2-WIRE TRANSMITTERS

AP4620-6XXX series, measuring 1.375 x 1.375 x 3.25" (3.49 x 3.49 x 8.26 cm), feature std thermocouple input connections and miniature "banana" plug connections for 4- to 20- or 10- to 50-mA current loop outputs. No special enclosures are required as they fit into conduit splice boxes. Featuring built-in cold-junction compensation and screwdriver-adjustable ZERO and SPAN, units can accept thermocouple probe assemblies directly. Devices operate in full −20 to 80°C industrial temp range off current loop supply voltages of 12 to 90 Vdc. **Action Instruments Co, Inc,** 8601 Aero Dr, San Diego, CA 92123.
Circle 241 on Inquiry Card

DISC CONTROLLER ADAPTER CARD

Able to connect the PerSci 1070 disc drive controller directly to any S-100 bus, the adapter card includes circuitry for an additional 3k bytes of EPROM and 1k bytes of RAM. These can be addressed at any 4k boundary in a systems memory by onboard jumpers. The controller mounts piggyback on the adapter and can be addressed to any I/O port by jumpers on the controller. Prototype area is supplied, as is circuitry for four 2708 EPROMs and two 2114 RAMs. **Info 2000,** PO Box 3196, Culver City, CA 90230.
Circle 242 on Inquiry Card

SHAFT-ANGLE ENCODER/INDICATOR

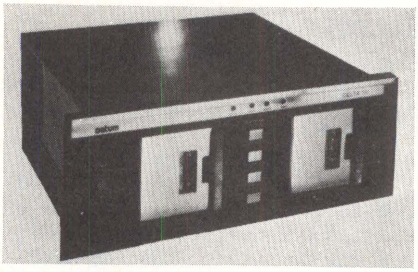


SR300, a low cost panel-mounting module, converts synchro or resolver data into a 4-digit unipolar (0 to FS) or bipolar (IFS) display and an equivalent DTL/TTL-compatible BCD output. The unit may be specified to be direct-reading in degrees of shaft rotation (0 to 359.90 or ±179.90), or optionally in engineering units for any parameter that can be linearly related to a shaft angle. Unipolar scales may have any FS value up to 999, and bipolar scales may have any FS value up to ±1999. **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
Circle 243 on Inquiry Card

SINGLE-PHASE UPS

AccuPac 1 delivers continuous, filtered precision power to critical loads and eliminates problems of power fluctuations or blackouts. Incorporating fully tested ICs, semiconductor devices, and built-in status switch for automatic protection of the critical load, the UPS has a 3-step startup and shutdown sequence to minimize operator functions. A completely illuminated mimic flow diagram, keyed in six colors and coupled with the instrumentation, gives complete, continuous status of the system. **Westinghouse Electric Corp, Industrial Equipment Div,** Westinghouse Building, Gateway Ctr, Pittsburgh, PA 15222.
Circle 244 on Inquiry Card

CASSETTE I/O SYSTEM



Designed for the DEC PDP-11, DELTA 111 performs functions of the DEC PC-11 high speed paper-tape punch and reader, and is compatible with existing PDP-11 software. Unit has bidirectional searching and rewind; control and status registers are the same as the PC-11 with added features of ready status, tape rewinding, beginning of tape, end of tape, and online. With maximum storage capacity of >300k bytes/cassette, unit has data transfer rates up to 2600 bytes/s. Interface is via a unibus extender connector at rear of unit. **Datum, Inc,** 1363 S State College Blvd, Anaheim, CA 92806.
Circle 245 on Inquiry Card

MICROPROCESSOR ENGINEER

To be assigned to evaluating new technology components and determine the feasibility of using microprocessor hardware integration techniques for COBOL or other high level languages. Will be evaluating processor architectures toward defining one which is optimal in some sense for the execution of a prescribed instruction set.

A knowledge of microprogrammable microprocessor operation with design experience concerning architectural tradeoffs and microcode techniques.

This is a senior level position in our Advanced Development group offering a high contribution and visibility environment.

REAL TIME SYSTEMS ENGINEERS

The candidates will review, analyze and propose requirements for common real-time system processor communications and peripherals for retail products. They will interact with other corporate and divisional groups for corporate commonality. They will provide consultation to the system/product designer on industry standards interpretation and adherence needs. Generates guidelines on communications and peripherals usage in Retail Systems.

From 3-10 years experience with a BS in Electrical Engineering, Systems Engineering or Computer Science is required; and MS is desirable. Knowledge of one or more of ANSI (ISO) standards on communications cassette, Disk, File formats, peripheral interfaces, code SETS and E.F.T. is very desirable.

We invite your response as soon as practical.

NCR

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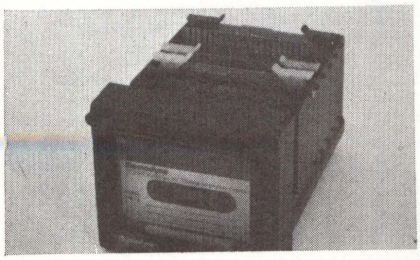
Robert W. Donovan
Terminal Systems Division—Cambridge
NCR Corporation
Box 728
Cambridge, Ohio 43725
614/439-0291

INDUSTRIAL/MILITARY ENERGY MONITOR



Model 30 performs mathematical computations relative to energy use while continuously monitoring electricity consumption. It compares usage rate to budgeted rate, and alerts personnel when rates are excessive; it sets off audible or visual alarms when consumption nears preset levels. Readings are displayed on a 5-digit LED readout. Options include a printer for hard copies; BCD output for data logging interface with automatic print intervals of 1 min, 1 h, 1 day; and power demand as well as power factor meters. **Franklin Electric Co, Programmed Power Div,** 995 Benicia Ave, Sunnyvale, CA 94086.
Circle 246 on Inquiry Card

ANSI/ECMA-COMPATIBLE RECORDER



Model 819-34 is a small, lightweight, low power recorder consisting of an incremental digital transport to which is mounted a card cage housing a write step card, a formatter card, and an I/O card containing a cyclic redundancy check (CRC) generator. An A-D converter and a 16-channel multiplexer card may also be added. Standby power requirement is 20 μW; while recording the unit requires only 500 mW. The recorder features a parallel input of up to 32 bits, a data rate of 50 bits/s, and a formatted capacity of 1M bits. **Memodyne Corp,** 385 Elliot St, Newton Upper Falls, MA 02164.
Circle 247 on Inquiry Card

LOW INERTIA DC MOTORS

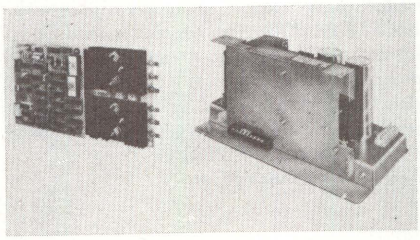
Totally enclosed, the small, flat motors provide a high torque to inertia ratio. Because of low inertia, they reach max speed in <20 ms, give constant high torque with a high peak torque rating, and have a reversible high speed feature. The variable speed units are offered in eight std types from 0.25 to 13 hp. They are rated at 3000 r/min and run from 4000 to 10,000 r/min. **Mavilor Motors, Div of Nuclear & Environmental Protection, Inc,** 285 Murphy Rd, Hartford, CT 06114.
Circle 248 on Inquiry Card

CUSTOM OPTIONS FOR DIABLO PRINTER

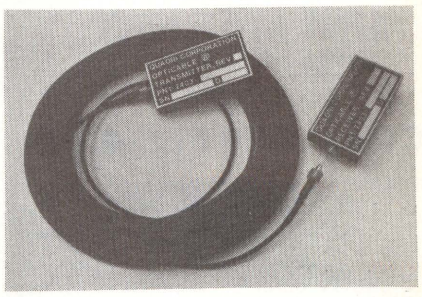
A 20-mA current loop interface for mini and microcomputer applications is available as an option for the Diablo 1620 printer. Also available is a custom-designed stand that is color matched to the terminal; the stand features a right-hand collapsible workshelf, ball casters, and a paper put-out basket. **Data Access Systems, Inc,** Dept SW, 100 Rte 46, Mountain Lakes, NJ 07046.
Circle 249 on Inquiry Card

STEPPING MOTOR MODULAR DRIVES

Modular translator and preset indexer drives for Slo-Syn stepping motors are offered with rates to 5000 steps/s, some with optional power supplies. Translator modules provide sequencing and switching logic for bidirectional control of motors. They convert pulses from external logic sources into a switching sequence needed to drive the motors the desired rate, direction, and number of steps. Types are available for 1000-, 3000-, and 5000-steps/s. **The Superior Electric Co,** 383 Middle St, Bristol, CT 06010.
Circle 250 on Inquiry Card



FIBER OPTIC DATA CABLE



Using IR light as its transmitting medium, model 2403 features easy installation (receiver and transmitter each plug into a DIP socket), TTL interface, 5-V operation, easy disconnection of cable, and data rates from dc to 2.5 MHz. Lengths are available from <1 to 100 ft (0.3 to 30.4 m). The 1.15 x 2.15 x 0.35" (2.92 x 5.46 x 0.89 cm) size enables units to be used on 0.5" (1.27 cm) card spacing. Cable is immune from electrical interference throughout its length and will not radiate during operation. **Quadri Corp,** 1725 W Seventeenth St, Drawer 2H, Tempe, AZ 85282.
Circle 251 on Inquiry Card

ROYTRON™
plug-compatible punch

Desktop punch with serial asynchronous RS-232C compatible interface. Designed to utilize ASCII defined control codes and operate with a terminal device on the same serial data lines. Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batched, utilizing a 32 character buffer.

Two modes of operation are provided: *Auto Mode* — Simulates Model ASR 33 Teletype punch using ASCII defined data codes (DC 2 and DC 4) to activate/deactivate the punch; *Manual Mode* — Code transparent mode. Panel switches control activation/deactivation of punch and associated terminal device.



MODEL 1060-AS
High-speed, compact, with self-contained electronics and power supply. Complete in attractive noise dampening housing.

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IN U.K. — ADLER BUS. SYSTEMS/OEM PRODS., Airport House, Purley Way, Croyden, Surrey, England
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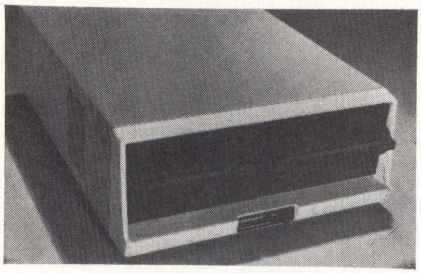
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PRODUCTS

FLOPPY DISC STORAGE SYSTEM



Available for 110-Vac, 60-Hz, or 220-Vac, 50-Hz operation, EXORdisk II consists of a dual side-by-side diskette drive unit, controller module, software package (MDOS), cable assembly, and support documentation. It provides 512k bytes of nonvolatile memory on two diskettes. Recorded data format is compatible with that of IBM 3740. The controller module is bus compatible with an EXORciser or Micromodule-based system, interfacing directly with the bus of either system. **Motorola Semiconductor Products, Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 252 on Inquiry Card

MINIATURE PIN-AND-SOCKET CONTACTS

Stamped-and-formed crimp removable contacts with 2-tine spring design for microminiature rack-and-panel, strip, and circular connector applications, Econo-Tac™ 220 series fit into a range of high and low density, plug and receptacle insert configurations offered in the company's 220, 221, 222, and 223 series connectors. Carrier reels can accommodate up to 20,000 contacts. Std plating is gold over nickel; current rating is 3 A. Devices accommodate 24-, 26-, and 28-gauge solid and stranded wires. **Amphenol North America Div, Bunker Ramo Corp,** 900 Commerce Dr, Oak Brook, IL 60521.
Circle 253 on Inquiry Card

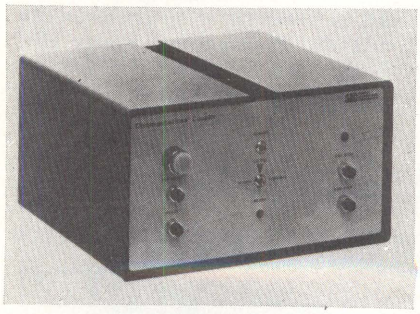
4800-BIT/S BELL-COMPATIBLE MODEM

A 4800-bit/s modem that is fully Bell-208 compatible for both dial-up and private lines, model 7208 has an all-digital adaptive equalizer which affords maximum convergence and prevents drifts and other analog errors. Equalizer uses a mean-square algorithm which allows the local modem to continually re-optimize the equalizer without restarting the remote transmitter. No restriction is placed on the coding of data, as the transmitter contains a scrambler to randomize the transmit signal. **Tele-Dynamics Div of AMBAC Industries, Inc,** 525 Virginia Dr, Fort Washington, PA 19034.
Circle 254 on Inquiry Card

FLOPPY DISC CONTROLLER/INTERFACE

Designed around a MOS/LSI floppy controller chip, the BTC-101 is an IBM 3740 compatible floppy disc drive controller/interface for Interdata computers. Fully contained on a single half board, the unit is intended to handle from one to eight Shugart SA800 drives (or equivalent). Single sector reads and writes can be fully buffered. Device also formats and utilizes sector sizes from 16 to 4096. It requires 5 V from the CPU and is available with full 10-bit address decoding, and buffering up to 512 bytes. **BGL Technology Corp,** Warner Victory Centre, Suite 307, 6355 Topanga Canyon Blvd, Woodland Hills, CA 91367.
Circle 255 on Inquiry Card

PARALLEL-TO-SERIAL DATA CONVERTER

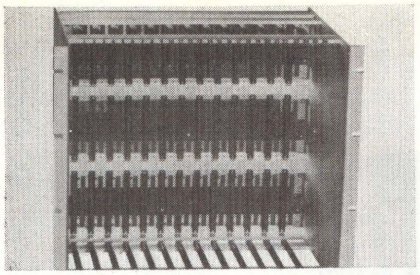


Model DC-6 accepts parallel input data and creates serialized output data which is compatible with nearly all std communications devices. The unit can be introduced into existing terminal-to-modem systems using normal software and without disturbing system configurations or capabilities. Input can be from almost any data collection or data generating device. Completely programmable and with an extremely flexible output format, the device consists of a chassis board for basic functions, plus plug-in boards to enhance capability. **Science Accessories Corp,** 970 Kings Highway W, Southport, CT 06490.
Circle 256 on Inquiry Card

REFRESHED GRAPHIC SYSTEM

Graphic option controller has the ability to generate and selectively erase picture elements for output to a raster scan display. When fitted to a conventional alphanumeric VDU, it forms a powerful interactive graphic terminal. Performance and versatility result from use of a hardware vector generator and microprocessor-based architecture. Full or dashed vectors may be drawn together with histograms and symbols on a matrix of 256 by 256 points. Graphic information can be superimposed on alphanumeric text from the VDU to form a composite picture. **Sigma Electronic Systems Ltd,** Church St, Warnham, Horsham, Sussex RH12 3QW, England.
Circle 257 on Inquiry Card

PANEL RACK ASSEMBLIES

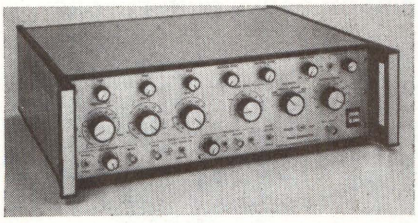


Family of panel rack assemblies and accessories, designed to complement 326 series panels, are available in 13 positions spaced on 1.2" (3.0-cm) centers, and can be expanded to 26 positions on 0.6" (1.52-cm) centers. A half rack accommodates six panels on 1.2" (3.0-cm) centers and 11 panels on 0.6" (1.52-cm) centers. Connectors can be easily removed from the power panel without having to desolder. Power panel may be removed for automatic or semiautomatic wirewrapping. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 258 on Inquiry Card

HIGH SPEED LINE VOLTAGE ANALYZER

Model LVA-110 can monitor line voltage with ½-, 1-, or 2-cycle time base. Each measurement is analyzed and compared against two memories which store the highest and lowest line voltage readings. Power Fail memory lights an indicator if power returns after interruption. Dynamic input range is 0 to 199 V; the analyzer can operate continuously over input power range from 50 to 160 V. Two optional output converters provide current source for 1-mA strip chart recorders with ranges of 80 to 140 V or 0 to 160 V. **Power-Science, Inc,** 8076 Engineer Rd, San Diego, CA 92111.
Circle 259 on Inquiry Card

BIPOLAR/MOS PULSE DRIVER



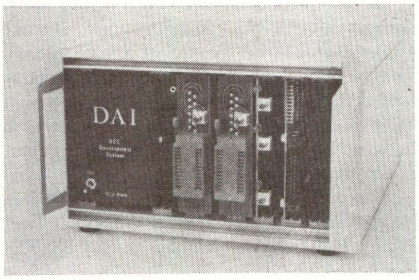
Model 136A general-purpose pulse generator provides low interaction between controls and low waveform distortion. Output circuit is a backmatched (internally terminated) 50-Ω source which provides up to 10 V into 50 Ω with fast risetimes required for bipolar testing. Unit is able to deliver up to 20 V into 50 Ω from a high impedance current source. Key specs include frequency rate of 10 Hz to 60 MHz; delay/width of 10 ns to 50 ms; *rise/fall* times, 3 ns to 8 ms; amplitude, ±20 V into 50 Ω; and offset rating of ±5 V. **E-H Research Laboratories, Inc,** 515 11th St, Box 1289, Oakland, CA 94604.
Circle 260 on Inquiry Card

CRT DISPLAY INTERFACE

VIURAM-8, video interface unit random-access memory for PDP-8 minicomputers, includes software for screen editing and requires only a single slot in OMNIBUS. Display format is 12 lines by 80 char/line. There are 128 displayable char including the USASCII 96-char set and 32 special symbols. Char matrix is 7 dots wide by 12 raster lines high. It has a high speed, static n-MOS RAM with 1k words by 12 bits/word and full R/W capability. Video display circuitry is fully buffered from the memory section. **Computer Technology,** 6043 Lawton Ave, Oakland, CA 94618.
Circle 261 on Inquiry Card

INTEL 2716 EPROM PROGRAMMER

Programming Intel 2716 EPROMs in 100 s, the 276 programmer is based on the DCE-2 microcomputer. It can also act as a standalone EPROM copier or verifier of



p/ROM-erased condition, and is compatible to any usual terminal (TTY, VDU) with V24 or 20-mA asynchronous interface from 110 to 9600 baud. Full paper tape I/O and memory commands include simple instructions for programming and flexible commands for data manipulations. Microprogram automatically performs compare operation after programming and lists programming errors if any. 2k EPROM memory space is available to add special functions. **Data Applications International,** Drève des Renards 6, Bte 8, 1180 Brussels, Belgium.
Circle 262 on Inquiry Card

100M-BYTE DISC SYSTEM

Model 3000/80 features an instruction set similar to IBM 370, and 32k bytes of high speed core memory. It contains an auto-answer modem for remote diagnostic support and data entry, a keyboard printer terminal, and two 50M-char disc drives with high speed data transfer. All interfaces and controllers are included for operation of basic peripherals. The fully-integrated business computer system is expandable to >1G bytes of online disc storage and up to 1M bytes of main core memory, and is able to support multiple terminals sharing a common data base and computer resources. **Advanced Information Design,** 745 Distel Dr, Los Altos, CA 94022.
Circle 263 on Inquiry Card

First in the Industry!
LEDs with PHOTOCONDUCTORS in DIP OPTO-ISOLATORS



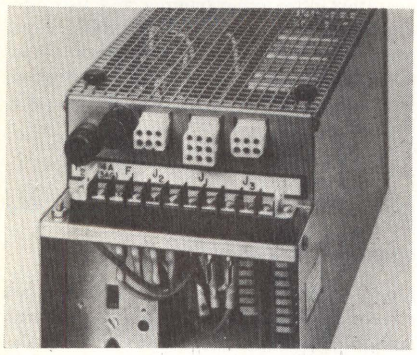
- For linear and logic functions
- High immunity to noise and transients
- 250V PAC output
- 1500 PAC isolation
- A-C input units utilize 2 LEDs in inverse parallel

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CLAIREX ELECTRONICS
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PRODUCTS

MULTIPLE OUTPUT SWITCHING POWER SUPPLY



A high efficiency, 3-output off-the-line supply for computer peripherals, microprocessor-based systems, multiplexers, modems, and minicomputers, OLS series offers three regulated outputs: 5 V at up to 24 A and ±12 V at up to 4 A each (total power out is limited to 172 W). All regulated outputs offer overvoltage and short-circuit protection. "Minimum holdup" of output voltages during power failure and full load with minimum input line is 50 ms. Input voltage is 115 or 230 Vac selectable, 47 to 63 Hz. **Powercube Corp,** 214 Calvary St, Waltham, MA 02154.
Circle 264 on Inquiry Card

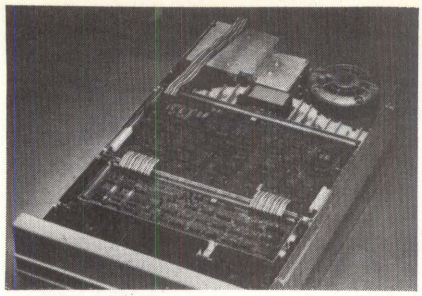
9-SEGMENT 1½-DIGIT INCANDESCENT DISPLAYS

MD-4N series Pinlite® incandescent displays with 0.25" (0.64-cm) char height and 0 to 19 readout incorporate the patented corner crossover technique for superior char definition. The 1½-digit configuration provides one full 7-segment digit plus a half digit, either decimal "1" or blank. Available in several voltage and current ratings, the displays are life rated at 100 kh/segment avg and provide up to 9k ftL brightness for readability in direct sunlight. They can also be filtered for a variety of colors. **Refac Electronics Corp,** PO Box 809, Winsted, CT 06098.
Circle 265 on Inquiry Card

17" GRAPHIC TERMINAL

Consisting of a 17" (43-cm) monitor, keyboard, and display electronics, model 801 provides a flicker-free display with 32 linear levels of gray scale on 4096 x 4096 addressable points. Video frame storage allows storage and display of a video image from a TV camera operating at the same line rate as the monitor; video images can be superimposed with computer generated images. Display electronics include character generator, vector generator, selective erase, and programmable function. **Princeton Electronic Products, Inc,** PO Box 101, North Brunswick, NJ 08902.
Circle 266 on Inquiry Card

DISC DRIVE

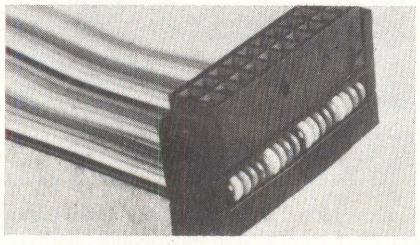


Reflex™ disc drive is available in three versions with one, two, or three disc platters providing 12.5M, 37.6M, or 62.7M bytes of storage in a 7" (17.78-cm) high rack-mountable package. Characteristics include avg head positioning time of 30 ms (6-ms track-to-track); unit can be fitted with additional 0.5M bytes of faster head/track storage for scratchpad-type operations with an average access time of 10 ms. Disc rotation speed of 3000 r/min results in average latency of 10 ms and data transfer rate of 7.08 MHz. **Microdata Corp,** 17481 Red Hill Ave, Irvine, CA 92714.
Circle 267 on Inquiry Card

ROTARY SWITCH FOR MINIATURE POTENTIOMETERS

Series 900 miniature potentiometer/switch combination, designed for snap-in installation, is rated at 6.5 A at 1.5 Vdc, 0.2 A at 45 Vdc. Overall mounted dimensions are 0.875 x 0.5" (2.22 x 1.27 cm). Hot stamped numbers are available on the colored thumbwheel edge. Additional features include spst NO or NC switch actuation at CW or CCW end; life of 25,000 operations at rated load; 3 in-oz (0.021 N•m) throw torque; and snap action. **Centralab Electronics Div, Globe-Union Inc,** PO Box 858, Hwy 20 W, Fort Dodge, IA 50501.
Circle 268 on Inquiry Card

RIBBON CABLE CONNECTORS



An insulation-displacement box contact on the 4700 series displaces cable insulation, cleans the conductor through wiping force, and terminates to the conductor without severing the wire or strands. No prestripping of flat cable is required. Dual wiping cantilever beams provide redundant electrical contact with either square or round 0.025" (0.064-cm) pin or headers. Housings are available in 10, 14, 16, 20, 26, 34, 40, 50, and 60 contacts. Options include recessed cover and strain relief. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.
Circle 269 on Inquiry Card

DIGITAL RECORDER



- Low cost, high reliability, compact
- One supply, 2 moving parts, excellent speed control
- Full electronics, TTL I/O, Auto-Sync® phase encode/decode
- Short IRG, 5.7 megabits, 8K Baud

Model CS-400A

BRAEMAR COMPUTER DEVICES, INC.

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BURNSVILLE, MINNESOTA 55337
(612) 890-5135

CIRCLE 85 ON INQUIRY CARD

DIP REED RELAY

Model 230 is designed for dc coil voltages to 24 Vdc; can be interfaced directly with RTC, DTC, TTL, and HTL logic circuits; and is IC compatible. Contact configurations are 1 Form A or 1 Form C for the 0.5-A model; 2 Form A for the 0.25-A version. Release time is 0.1 ms max. Avg (resistive) life expectancy is 5M operations for the 0.25-A model. Initial contact resistance is 0.15 Ω max at rated voltage. Terminals are DIL pin-type on std 0.100" (0.254-cm) grid spacing for PC boards. **Deltrol Controls/Div of Deltrol Corp,** 2745 S 19th St, Milwaukee, WI 53215.
Circle 270 on Inquiry Card

SILICON NPN POWER-SWITCHING TRANSISTORS

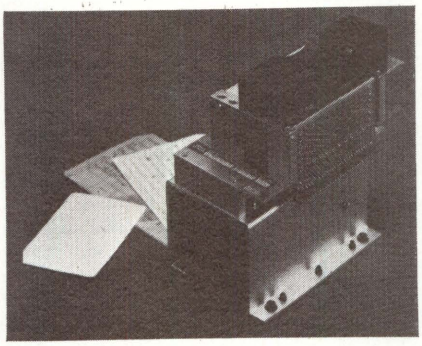
High current, silicon npn power transistors, 9113, 9113A, and 9113B, for use in offline power supplies and other high voltage switching applications feature high voltage capability (V_{CEO} = 400 V for 9113B), fast switching speeds (t_r = 1 μs and t_f = 0.75 μs), and low saturation voltages (V_{CE} (sat) = 1 V for 9113), together with high safe-operating-area ratings for both forward- and reverse-bias conditions. Specifically for use in offline switch-mode power supplies, units are supplied in a JEDEC TO-3 package. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876.
Circle 271 on Inquiry Card

HANDHELD LOGIC ANALYZER

The 45-B simultaneously displays four channels of digital logic waveforms on a conventional, single-trace scope, allowing observation of complex timing relationships. Relative input and output conditions can be verified; circuit operation with respect to clocks and various timing pulses can be observed. Battery permits portable operation. It can be used with a range of logic families, including TTL, DTL, RTL, and CMOS, without having to set threshold. **Digital Broadcast Systems, Inc,** 4306 Governors Dr, Huntsville, AL 35805.
Circle 272 on Inquiry Card

BADGE AND TAB CARD READER

For use as a data input device for computer or peripheral equipment, model 144 accepts 80-col tabulating cards as well as personal identification or badge type cards. Cards and badges may be read automatically in any sequence in the manually-fed, motor-operated unit. Reader outputs can be parallel binary, BCD, or Hollerith punched data from standard 80-col paper or plastic cards, manifold tab cards with carbon copies, and plastic ID cards. Reader measures 3.4 x 5.6 x 4.6" (8.6 x 14.22 x 11.9 cm) and weighs 3.5 lb (1.6 kg). **AMP Capitron Div,** Elizabethtown, PA 17022.
Circle 273 on Inquiry Card



TELECOMMUNICATIONS DISPLAY SYSTEM

Emulating IBM 3271 and 3275 display systems, the GT-70 system can accommodate up to 32 terminals and is available with all 3277 keyboard and display functions. Software uses IBM's binary synchronous communications discipline for 3270 systems at line speeds up to 9600 baud. Hardware is constructed from Data General minicomputers serving any combination of terminals with displays having speeds from 300 to 9600 baud, and printers operating from 30 char/s to 600 lines/min. Program can be configured to run under three operating environments: standalone, mapped, or unmapped disc-based systems. **Gamma Technology,** 800 Welch Rd, Palo Alto, CA 94304.
Circle 274 on Inquiry Card

The Inforex 180 Magnetic Line Printer.
Only the paper is ordinary.

Our patented dry-ink transfer gives you a high quality printout on an ordinary, inexpensive 8½" roll of paper. But everything else about the 180 is definitely *not* ordinary.

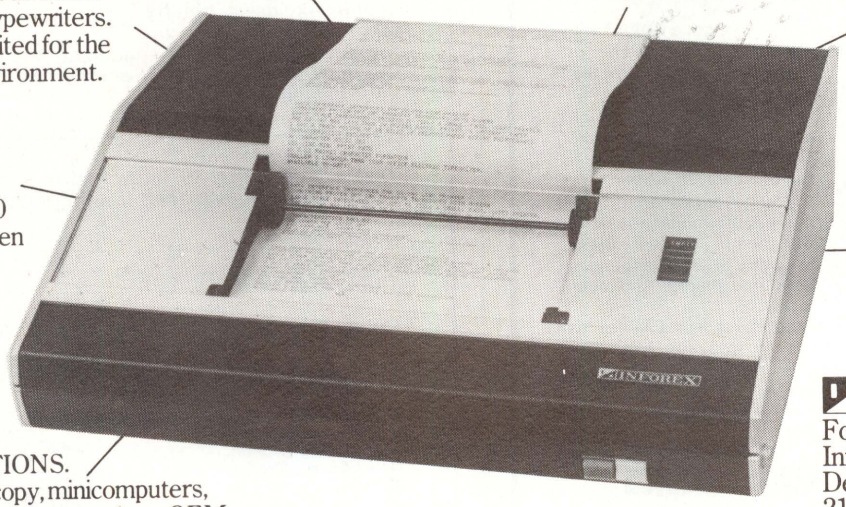
QUIET.
At least 10db below electric typewriters. Ideally suited for the office environment.

SMALL.
Desk top size, weighs just 33 pounds.

INTERFACE.
Serial RS-232 or TTL. Parallel TTL.

CHARACTER SET.
Full 96 characters ASCII, upper and lower case. Expanded character sets available as options.

FAST.
180 lines per minute. A 1920 character screen in 8 seconds.



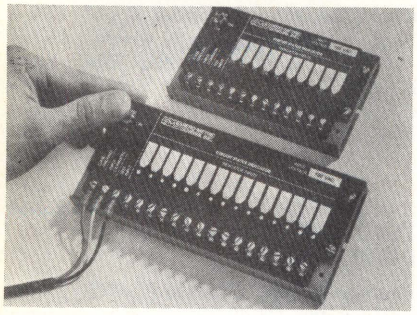
GRAPHICS OPTION.
Permits intermix of text with bar charts, curves, etc.

APPLICATIONS.
CRT hard copy, minicomputers, remote printing operations, OEM or end-user.

INFOREX
For more information, write Inforex, Incorporated, Dept. 588 CD-7, 21 North Ave., Burlington, MA 01803

PRODUCTS

CIRCUIT STATUS INDICATORS



For troubleshooting and monitoring electrical/electronic circuit functions, indicators display voltage status throughout a system. Standard 10- and 15-segment devices are available with LED or neon lamps. LED inputs are 5 to 50 Vac/dc or 120 Vac. Neon inputs are 120 Vac/dc or 240 Vac. All models have off-on-test (momentary) switch. Indicator nomenclature can be repeatedly written and erased. Sizes are 5.75 x 3.25 x 1.25" (14.61 x 8.26 x 3.18 cm) (10-segment) and 7.75 x 3.25 x 1.25" (19.69 x 8.26 x 3.18 cm) (15-segment). **Aero-Metric General, Inc,** 155 Franklin St, Dayton, OH 45402.
Circle 275 on Inquiry Card

SEVERE ENVIRONMENT MINICOMPUTER

A self-contained module consisting of four multilayer board logic modules, power supply, chassis, and control panel, SECS 111 is compatible with and emulates all functions of the DEC PDP-11/34 or /35. It is an industrial system designed for reliability and ruggedness. CPU is mounted on two boards, with I/O bus and an optional 1k words of RAM mounted on the other two boards. Additional board positions provide space for custom I/O, up to 32k words of p/ROM, and up to 128k words of semiconductor or core RAM. **Electronic Memories and Magnetics, Severe Environment Products Div,** 20630 Plummer St, Chatsworth, CA 91311.
Circle 276 on Inquiry Card

SCALABLE ABSOLUTE ENCODERS

With resolutions of up to 1 part in 1M and choice of 10, 64, or 100 turns for full count, DIGI-SHAFT units convert any shaft input to 5- or 6-digit BCD, or 16 bits of binary information corresponding directly to the shaft angle, with an accuracy of up to ±1 part in 100,000. In addition, 4-, 5-, or 6-digit 0.5" (1.27-cm) H LED displays of that angle are available. Shaft transducers are highly reliable resolvers. Data outputs are TTL-compatible; data transfer and data hold line provide simple com-



puter interfacing. Basic update rate is 2.5 ms. **Computer Conversions Corp,** 6 Dunton Court, East Northport, NY 11731.
Circle 277 on Inquiry Card

7-SEGMENT CHARACTER DISPLAY TUBE

Manufactured in sizes up to about 25" (63.5 cm) diag and displaying special characters, the 7-segment char display tube operates in a manner similar to a cathode-ray tube. A front faceplate carries a high luminance, high efficiency phosphor energized by a flood beam of electrons from the cathode. Placed between cathode and faceplate is a 7-segment mask with a lead from each segment brought out separately so they can be switched. With a control voltage swing of 5 V at 10-MΩ input resistance, only low level driving logic is required. Supply voltage is 12 Vdc; power consumption is 2 W for the 4" (10-cm) (E727) and 3 W for the 8" (20-cm) tube (E728). **English Electric Valve Co Ltd,** Chelmsford, Essex CM1 2QU, England.
Circle 278 on Inquiry Card

OS/8 Users:
Now you can get up to 16 users on a PDP-8 at the same time



If you've got a PDP-8* with an OS/8* operating system – or you're considering one – then you should talk to us.

We're Quodata. And our ETOS package takes a single-user OS/8 system and turns it into a multi-user OS/8 system.

You get time sharing, real-time and batch simultaneously. Full 32K memory for every user. Supports all OS/8 languages. Resource sharing. And much more.

For much less. Far less than it costs to add more PDP-8's.

So contact us: Educomp, subsidiary of Quodata Corporation, 196 Trumbull Street, Hartford, Conn. 06103. (203-728-6777)

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Specialists in DEC software

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Company_____

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City, State, Zip_____

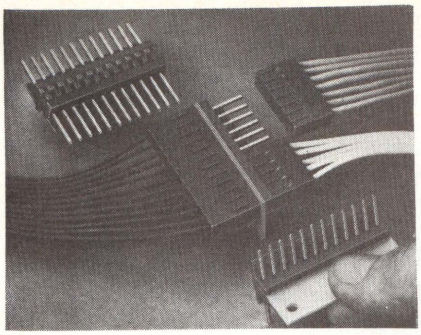
Mail to: George Sahl,
Gates Energy Products, Inc.
1050 S. Broadway, Denver CO 80217

CD-7

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CIRCLE 87 ON INQUIRY CARD

PCB BULKHEAD CONNECTORS



Interfacing different size crimp contact receptacles on PC board bulkheads, "Double-Header" miniature Term-acon® connectors are available with in-line or right angle pin configurations with screw, rivet, or snap-in mounts, and in stacked arrays and extended configurations up to 24 pins. The 0.045" (0.114 cm) sq pins may be positively identified with a permanent legend on the connector body. Dielectric strength between adjacent terminals is 1500 V rms (60 s duration) and max rated voltage is 250 Vac. **Methode Electronics, Inc,** 1700 Hicks Rd, Rolling Meadows, IL 60008.
Circle 279 on Inquiry Card

CRT CORRECTION MODULES

C104/C104B are solid-state, nonlinear function modules which accurately correct for geometric (pin cushion) and focus distortion in flat and semiflat faced CRTs using magnetic deflection. Producing wideband corrected output functions for horizontal and vertical deflections plus dynamic focus, the compact units are easy to use, connecting between horizontal and vertical inputs in their deflection amplifiers. Models are available for total deflection angles up to 90 deg. Both modules feature bandwidths of 10 MHz, 400 V/μs slew rates, settling times of 400 ns (to 0.1%), and typ accuracies of 0.2% FS. **Intronics, Inc,** 57 Chapel St, Newton, MA 02158.
Circle 280 on Inquiry Card

CARD-MOUNTED POWER SUPPLIES

CD series regulated supplies mounted on 4.5" (11.43-cm) sq PC boards provide outputs ranging from 5 V at 1.5 A to 30 V at 0.42 A. It is available in 11 single- and two dual-output models. Dual outputs are $\pm$12 and $\pm$15 V at 0.42 and 0.37 A, respectively. Outputs are voltage-fixed and factory-adjusted to within $\pm$1%. Optional, accessible voltage control permits 5% adjustment on models providing outputs of $\leq$20 V and 1-V adjustment on those providing >20 V. On dual-output devices, optional adjustment controls both voltages which are fixed to within 1% of each other. **ACDC Electronics,** 401 Jones Rd, Oceanside, CA 92054.
Circle 281 on Inquiry Card

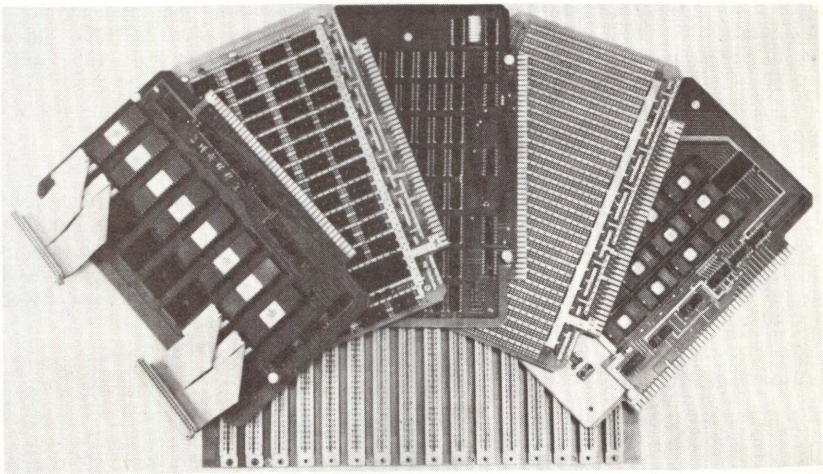
2- PAIR DATA BUS CABLE

Designed to carry data over long distances, the 150-Ω, low-loss YRS-15250 utilizes twisted pair construction with an overall Duofoil® (aluminum-polyester-aluminum laminate) shield enclosed in a black polyvinylchloride jacket. For ease of shield termination, a 22-gauge stranded tinned-copper drain wire is used, and is kept in constant shield contact. Color-coded cellular polypropylene insulation with a wall thickness of 0.045" (0.114 cm) covers each 22-gauge solid tinned-copper conductor. **Belden Corp, Electronic Div,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 282 on Inquiry Card

HIGH VOLTAGE POWER SUPPLY

Model 7000 series offers fast slewing rates of 50 V/μs over 8-kV range, and 240 V/μs over 6-kV range for commercial and military applications. Std features include subassembly modules for logistic support; compliance with MIL-Spec requirements of groundbase, shipboard, and avionic systems; UL conformance; arc and short-circuit protection; low ripple of 0.1% pk-pk, test points; and 10,000-h MTBF. Packaged in 9.5 x 5.75 x 2.8" (24.13 x 14.61 x 7.11 cm) capsules, devices are digitally programmable to five levels with output levels to 18 kV. **CPS, Inc,** 722 E Evelyn Ave, Sunnyvale, CA 94086.
Circle 283 on Inquiry Card

We'll Stack The Deck



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with our Family of EXORciser* compatible cards.

The 9600 Family of Support Modules is a set of generalized building block hardware designed around the M6800 Microprocessor. The cards are pin and outline compatible with the Motorola EXORciser* and Micromodules,* the MEK6800D1 and MEK6800D2 Evaluation Kits, and with other industry standard cards.

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9615	4K Erasable PROM Module	350.00	210.00	NOW
9615K	4K EPROM Kit of Parts	275.00	165.00	NOW
9620	16 Port Parallel I/O Module	375.00	225.00	NOW
9626	8K Static RAM Module	350.00	210.00	NOW
9626K	8K RAM Kit of Parts	275.00	165.00	NOW
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LITERATURE

Solid-State Relays

Two-color folder furnishes applications, specs, features, dimensional drawings, and graphs for line of mini and micro cube solid-state relays. **Grayhill, Inc,** La Grange, Ill.
Circle 300 on Inquiry Card

Fluorescent Indicator Panels

Selection guide comprised of color photos and wiring diagram lists advantages, modes and theory of operation, and complete charts of specifications for FIPs. **NEC America, Inc, Electron Devices Div,** Santa Clara, Calif.
Circle 301 on Inquiry Card

Small Computers

Complete with applications, color catalog discusses systems, personality modules, software, memories, disc storage, interfaces, and peripherals. **Processor Technology Corp,** Emeryville, Calif.
Circle 302 on Inquiry Card

Thermal Printers

Catalog contains special features, specs, photo, I/O connector pin assignment and data coding charts, interface description, and outline drawing of the 7-column thermal numeric printer. **Gulton Industries, Inc, Measurement & Control Systems Div,** East Greenwich, RI.
Circle 303 on Inquiry Card

p/ROMs

As an aid to selecting and using p/ROMs and related support equipment, guide covers usage tips on bipolar, MOS, and TTL bipolar devices, and contains a selection guide in chart form. **Pro-Log Corp,** Monterey, Calif.
Circle 304 on Inquiry Card

Magnetic Media

Brochure discusses history, current applications, and future potential for removable magnetic data and word storage devices. **Information Terminals Corp,** Sunnyvale, Calif.
Circle 305 on Inquiry Card

DIP Reed Relays

Two-page chart which tabulates complete characteristics of line of DIPs highlights catalog providing application data, graphs, and dimensional drawings for devices. **Magnecraft Electric Co,** Chicago, Ill.
Circle 306 on Inquiry Card

Data Communications Systems

Specs for three packaged systems are included in colorful brochure which lists configurations for use in such applications as data concentration, packet-switching, and remote batch processing. **Interdata, Inc,** Oceanport, NJ.
Circle 307 on Inquiry Card

Interface Bus

Brochure, offering concise explanation of instrument/computer interfacing and product evolution, contains applications, options, accessories, and bibliography for HP-IB implementation of IEEE Std 488. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 308 on Inquiry Card

Linear Power Supplies

Presenting detailed specs and photos, short-form catalog covers company's line of single, dual, and triple output, UL approved dc microprocessor power supplies. **ACDC Electronics, div of Emerson Electric Co,** Oceanside, Calif.
Circle 309 on Inquiry Card

Regulators

Leaflet and two papers cover all aspects of minicomputer regulators including features, selection information, and protection from errors. **Sola Electric, div of Sola Basic Industries,** Elk Grove Village, Ill.
Circle 310 on Inquiry Card

Mass Termination Connectors

Data sheet contains features, specs, dimensional drawings, and tooling information pertaining to Lace-N-Lok wire to post connectors designed for mass termination. **AMP Inc,** Harrisburg, Pa.
Circle 311 on Inquiry Card

Circuit Protection

Complete specs, dimensional drawings, and time-current characteristics graphs are features of catalog presenting circuit protection devices, relays, switches, buzzers, and flashers. **Littelfuse, Inc,** Des Plaines, Ill.
Circle 312 on Inquiry Card

Transportation Automation

Illustrated report looks at solutions to shipping documentation by means of advances in computer and telecommunication technology, and discusses potential of a world trading community linked by data networks. **Computer Sciences Corp,** El Segundo, Calif.
Circle 313 on Inquiry Card

Switch Applications

Fully illustrated publication concerned with sensing and control functions describes seven switch applications and offers a compact review of solid-state sensing. **Micro Switch, div of Honeywell,** Freeport, Ill.
Circle 314 on Inquiry Card

Universal Connector

Foldout bulletin explaining the cage jack concept covers applications, features, insertion and extraction forces, electrical properties and ratings, and environmental testing. **Cambridge Thermionic Corp,** Cambridge, Mass.
Circle 315 on Inquiry Card

Magnetic Shielding

Operating parameters, characteristics, and applications of METASHIELD™ fabric are featured in brochure containing small sample of product. **Allied Chemical, Metglas Products,** Florham Park, NJ.
Circle 316 on Inquiry Card

Potentiometers

With a reference section providing definitions, a summary of MIL-R-22097 requirements, and a review of applications, catalog offers complete specs and circuit diagrams for military and general-purpose cermet trimming potentiometers and panel mounting adapters. **Beckman Instruments, Inc, Helipot Div,** Fullerton, Calif.
Circle 317 on Inquiry Card

Data Conversion

The Analogic Data Conversion Systems Digest, Edition 1, contains parametric definitions and design considerations, state-of-the-art, and applications of ADCs and DACs, as well as a design reference guide, cross reference index, and bibliography. Price is $10.50. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.

Automatic Test Equipment

Illustrated catalog describes line of equipment with separate presentations, each including a general description, primary applications, and basic features. Write on company letterhead to: **Teradyne, Inc, Publications Dept,** 183 Essex St, Boston, MA 02111.

Magnetic Bubble Devices

Computer Science & Technology: Foreign and Domestic Accomplishments in Magnetic Bubble Device Technology assesses the status of the technology, and describes accomplishments, technical and economical factors, and applications. Price of SD Cat No C13.10:500-1 is $1.10. **Superintendent of Documents, U.S. Government Printing Office,** Washington, DC 20402.

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